

Radiation Tolerant Computing for Aerospace Applications

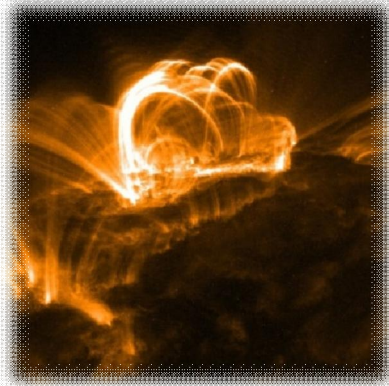
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Motivation

Radiation-Hardness for Aerospace Systems



- Cosmic radiation induces transients in integrated circuits
- Commercial processes are susceptible to Single-Event-Upsets (SEUs)
- Aerospace systems must address this additional constraint

Mitigation Techniques

- A variety of approaches are used to achieve radiation-hardness:

1) Radiation by Architecture

- *Triple Modulo Redundancy, Fault Recovery Processes, COP*

2) Radiation by Design/Process

- *Substrate doping, Enclosed Layout Transistors, isolation trenches*



Motivation

Hasn't this been solved?

- Manned Missions Have Been Underway for 50 years

Mercury

1958-1963

(put a man in orbit)



Atlas

Gemini

1965-1966

(long duration in space)



Titan II

Apollo

1968-1975

(put a man on the moon)



Saturn V

Space Shuttle

1975+

(sustained space presence)



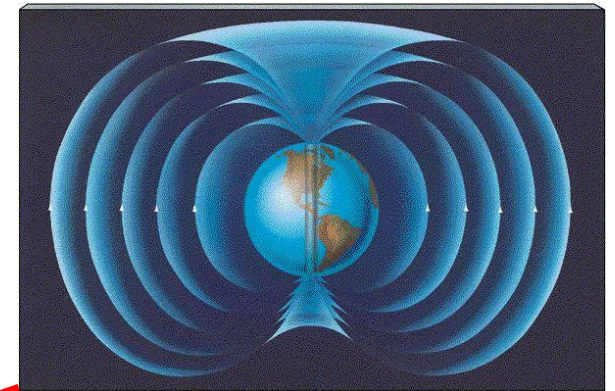
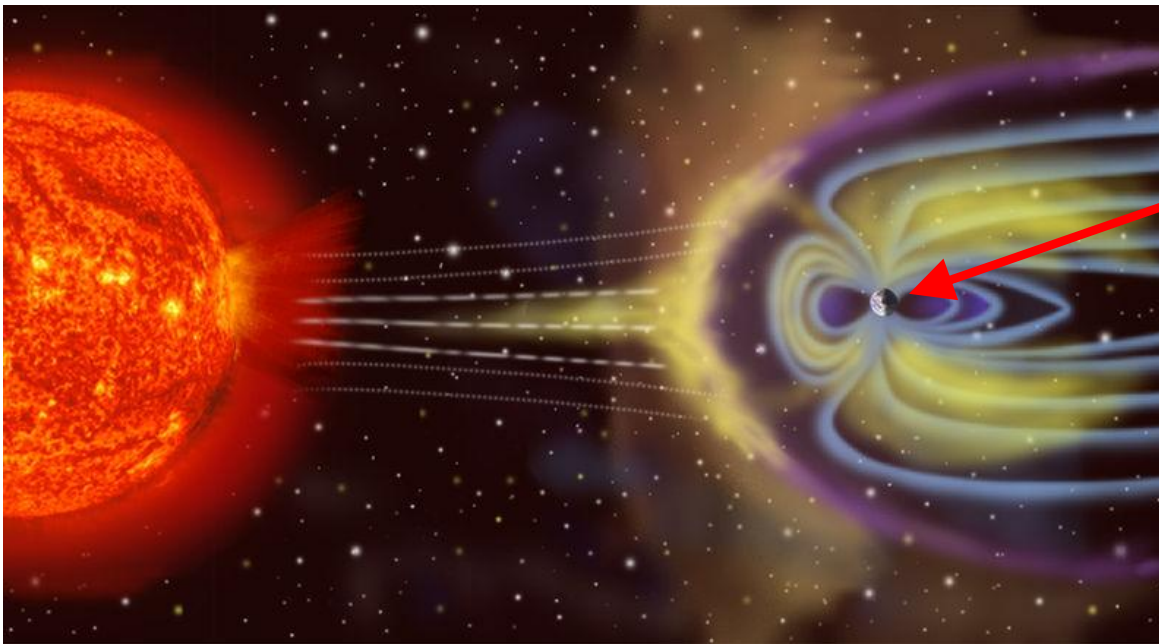
SRB + O₂/H₂ Tank



Motivation

Hasn't this been solved?

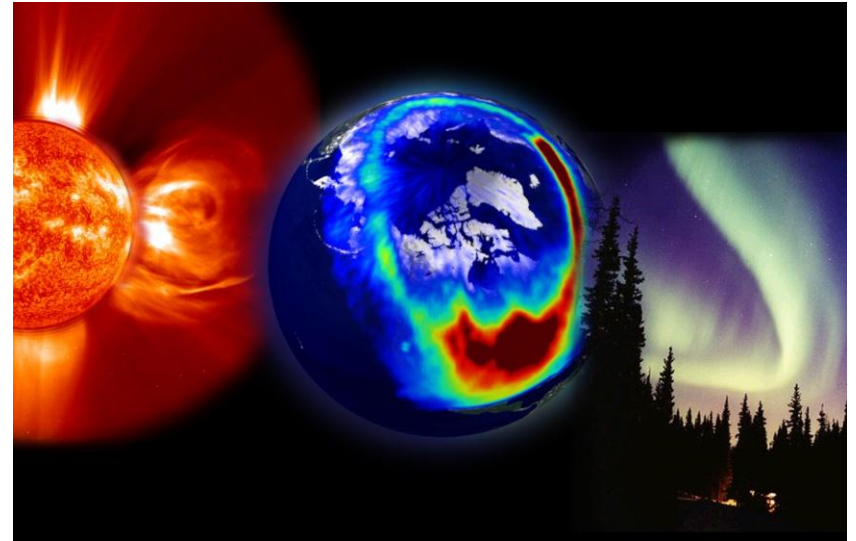
- Missions to Low Earth Orbits are protected from Radiation by the Earth's Magnetic Field



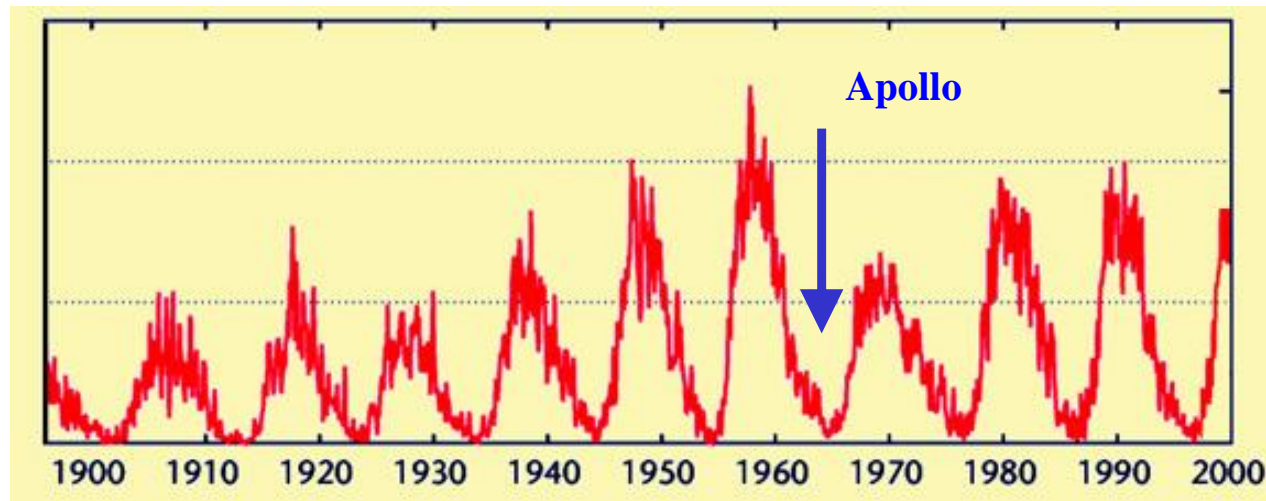
Motivation

How Did Apollo Do It?

- Solar events which cause major radiation occur in 12 year periods
- Apollo was timed to occur between solar events



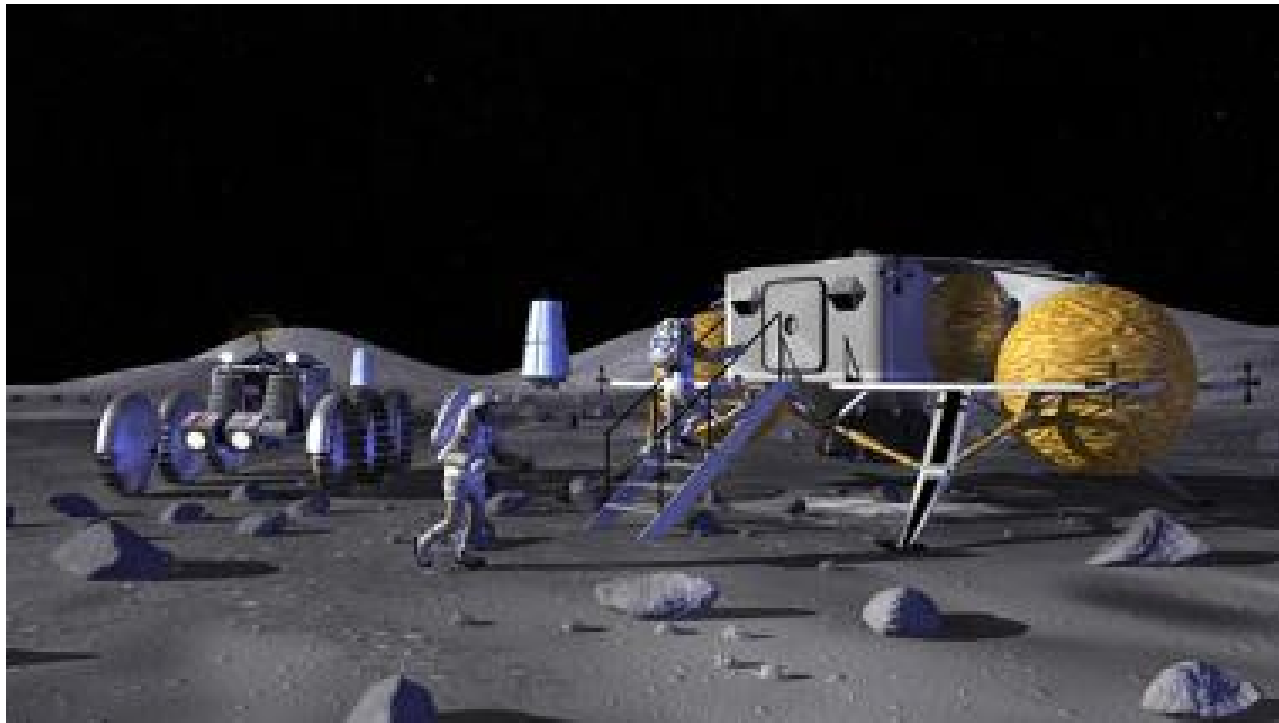
**Solar
Activity**



Motivation

Why not time it again?

- it's a different mission now, we want 10 yrs + outside of the magnetosphere



Lunar Surface Systems



Motivation

Constellation – the next generation...



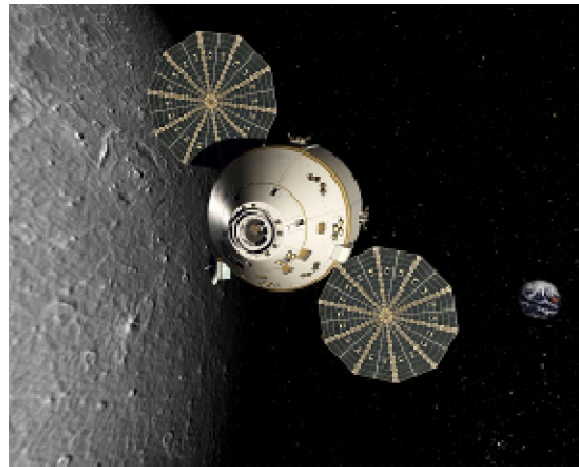
Ares I & V Launch Vehicles



Concept image of the Ares V Earth departure stage in orbit, shown with the Orion capsule docked with the Altair lander (NASA MSFC)



Altair Lunar Lander



Orion Crew Exploration Vehicle

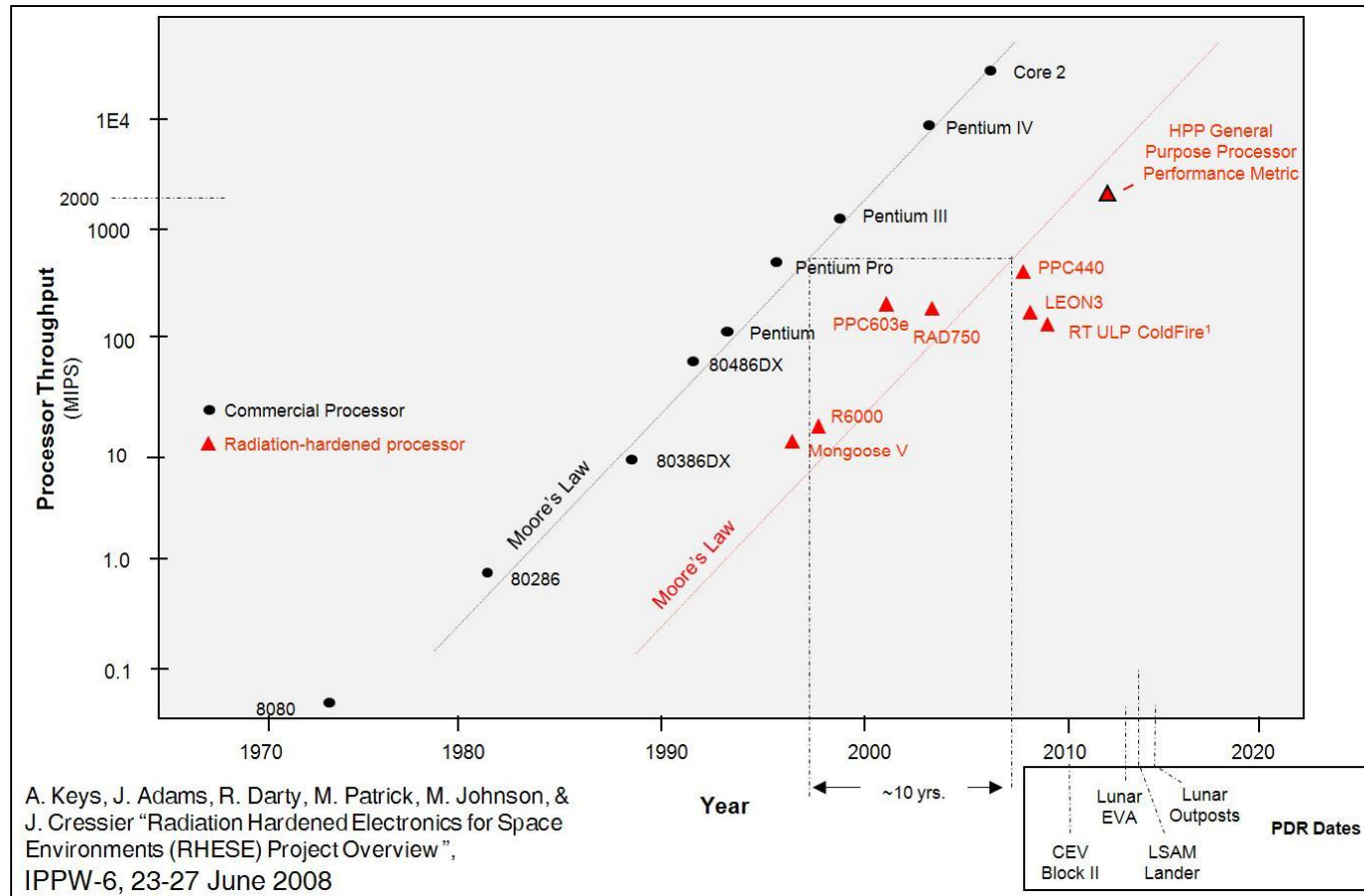


Orion Re-entry



Motivation

The Drawback of Rad-Hard Processors



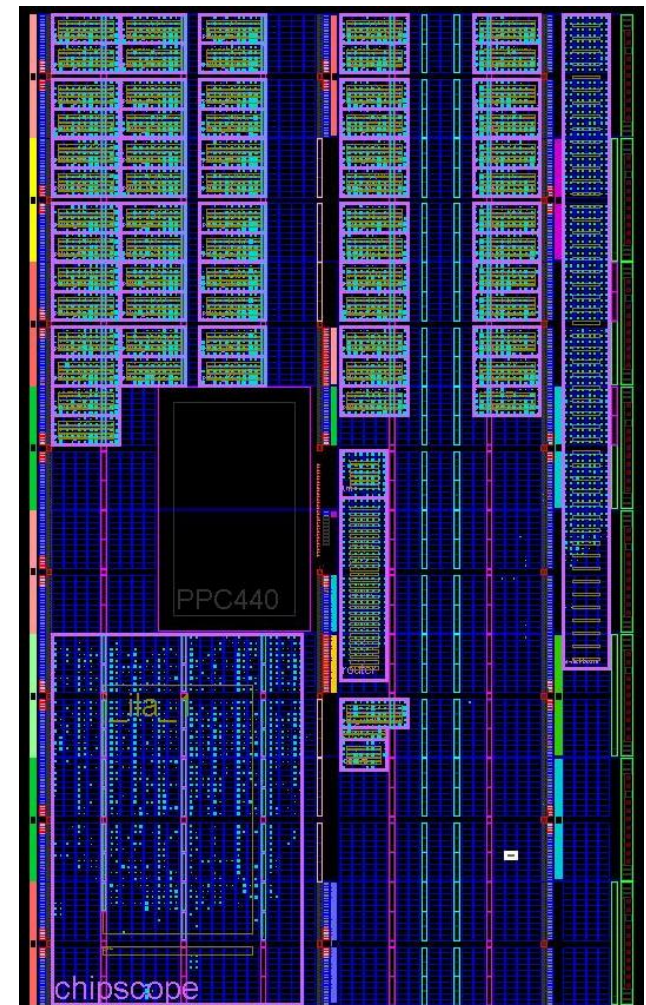
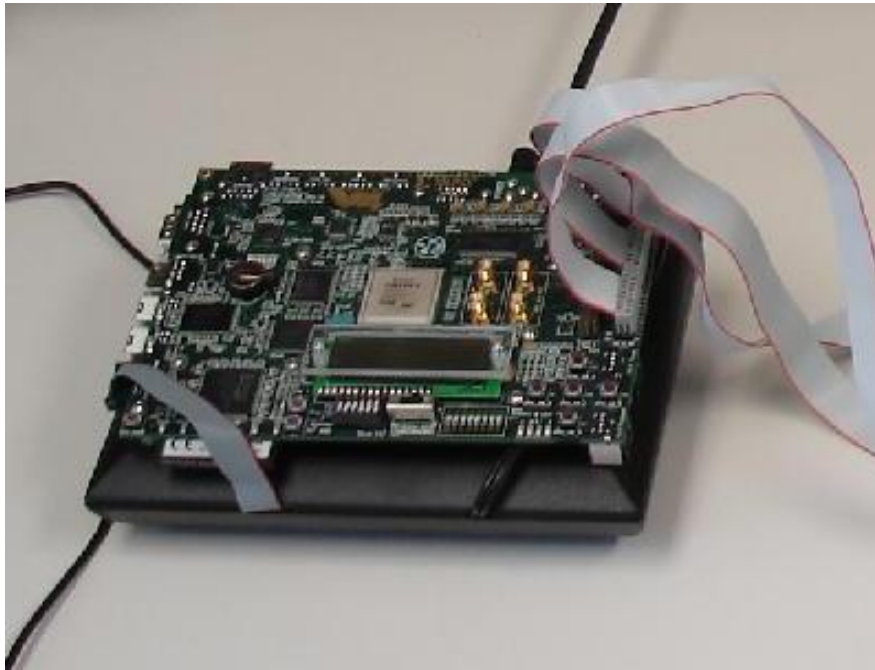
Radiation-Hardness translates into slower performance and more power consumption



Our Approach

Spatial Avoidance of Radiation Strikes Using Programmable HW

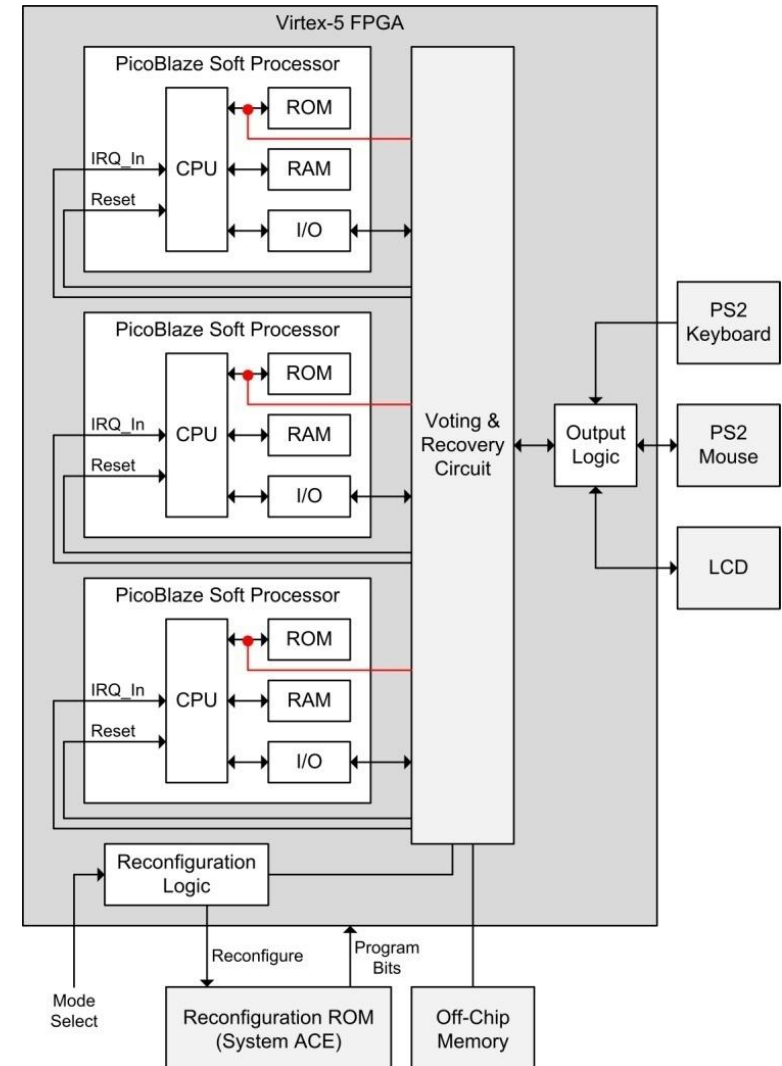
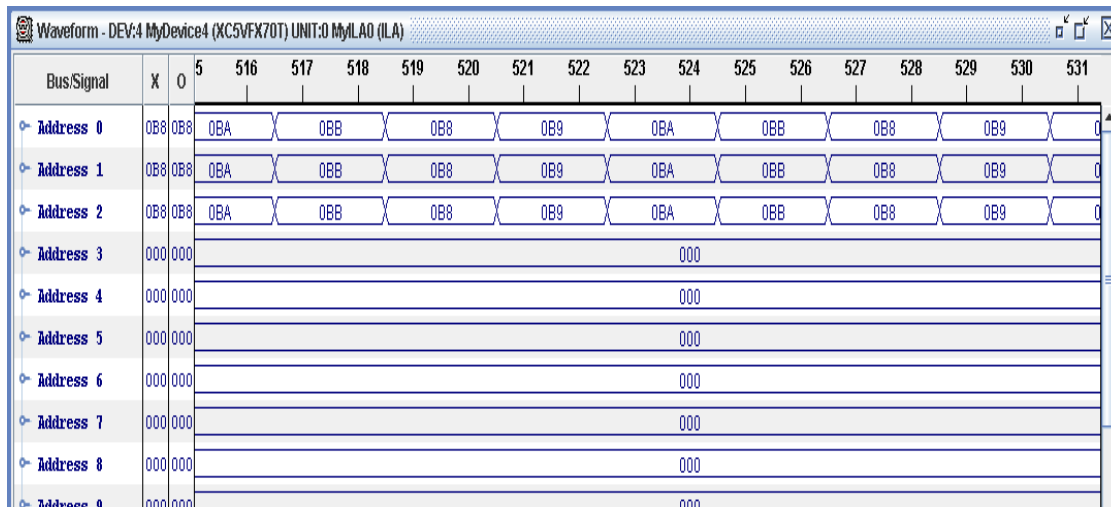
- Redundant Processors (spares)
- Real Time Reconfiguration



Our Approach

Three Processors Run in Synchrony

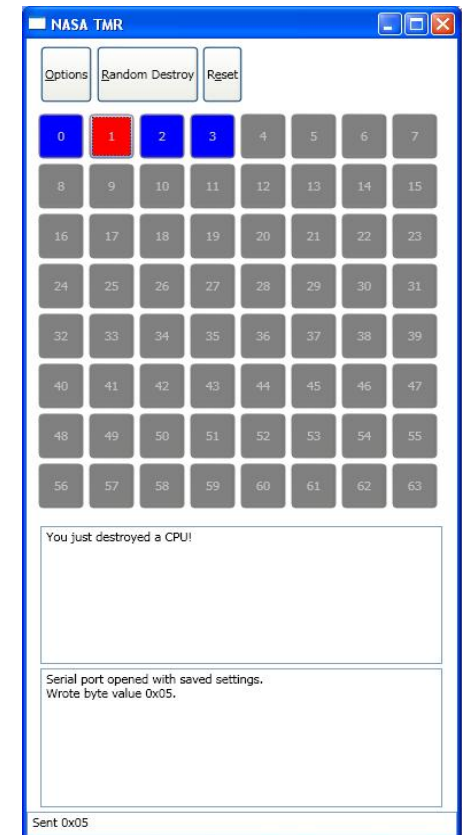
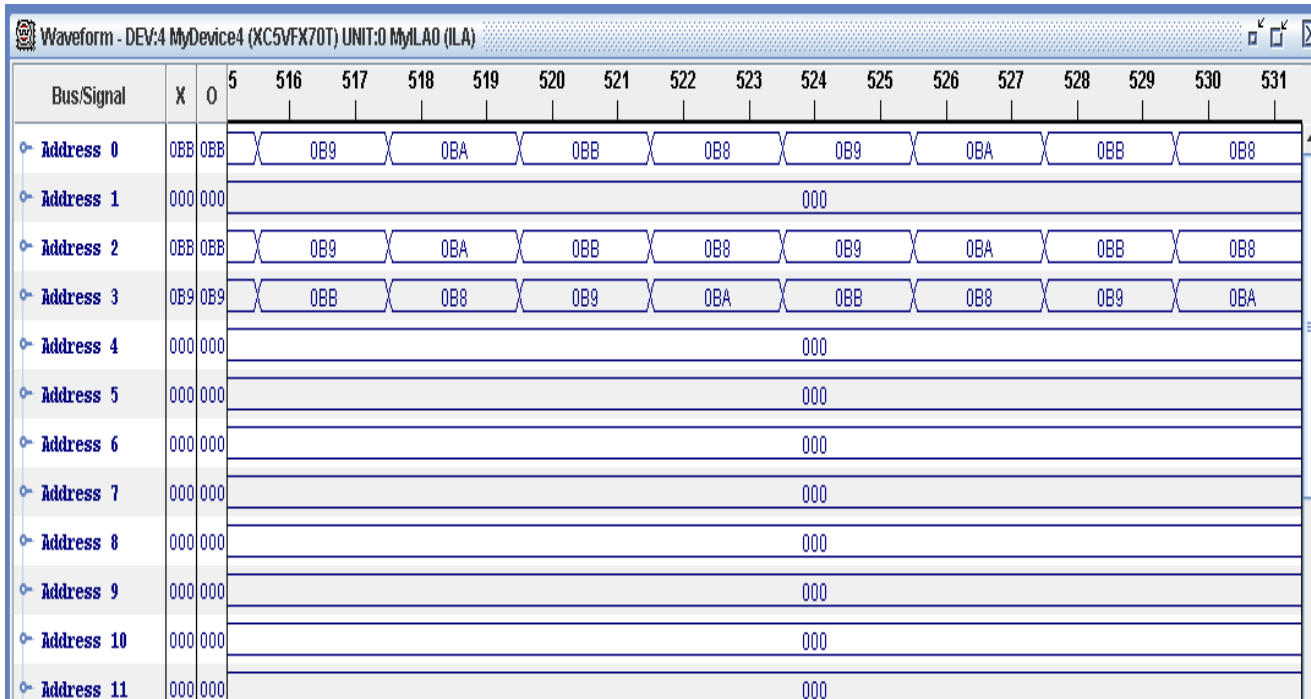
- Triple Modular Redundancy (TMR)
- Voter Circuit Checks for Errors



Our Approach

If Errors Are Detected in a Processor, Another One is Brought Online

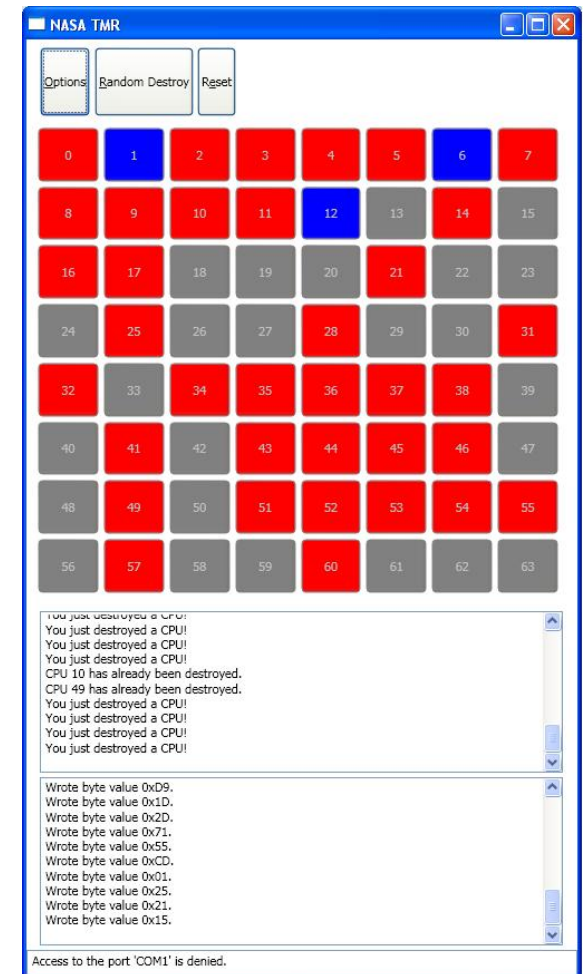
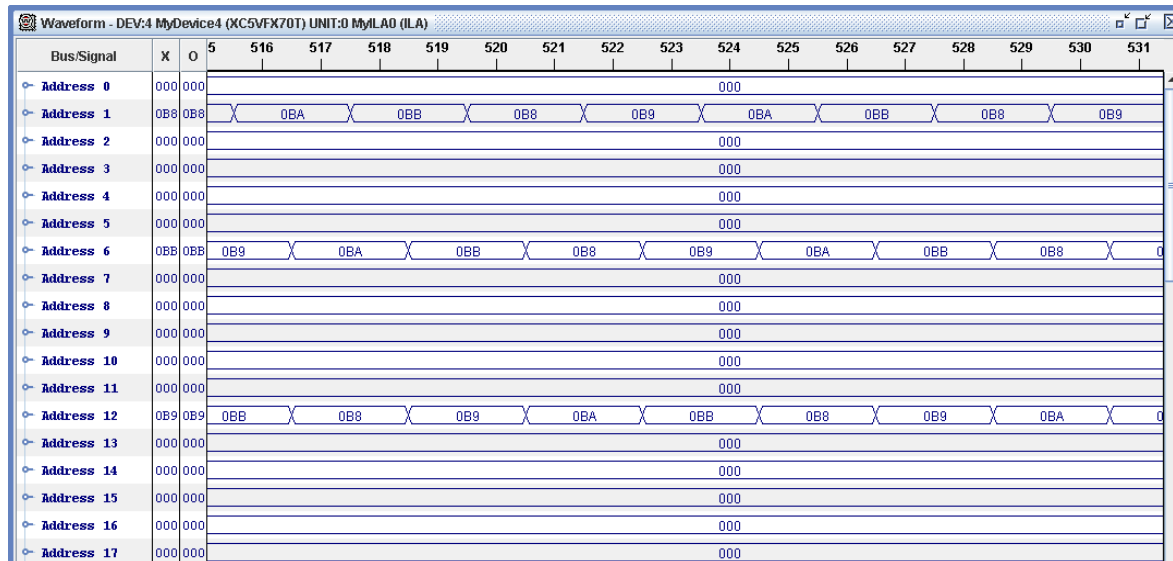
- TMR is still in tact



Our Approach

System Continues to operate in the presence of radiation

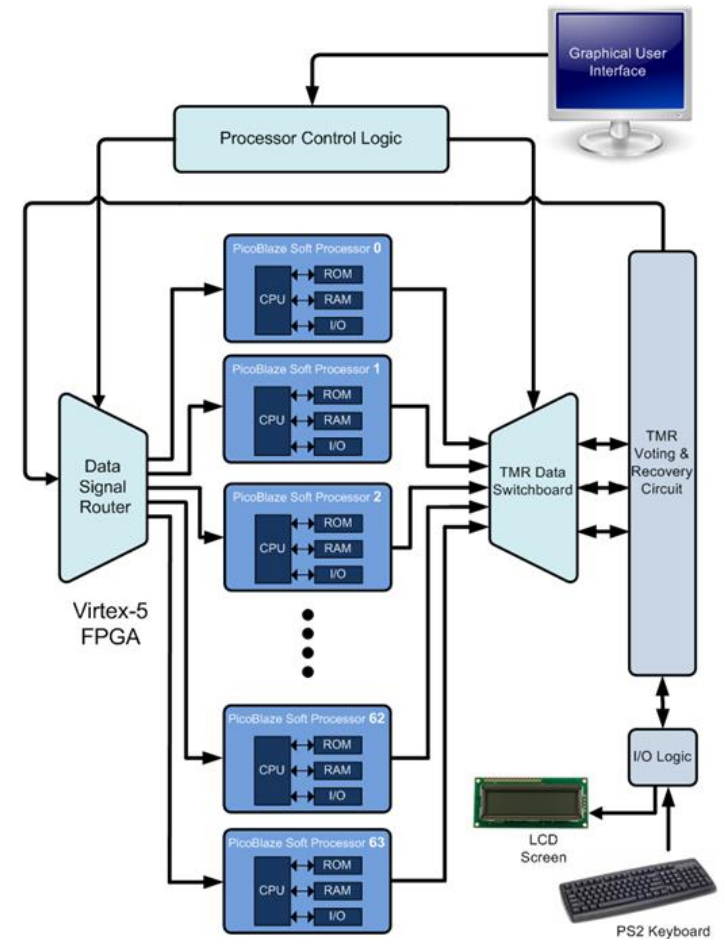
- Damaged regions can sometimes be repaired.



Our Approach

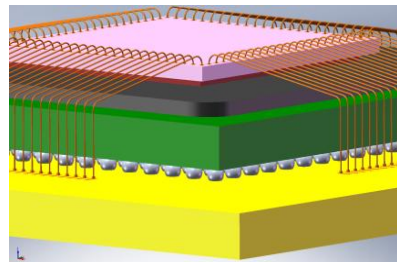
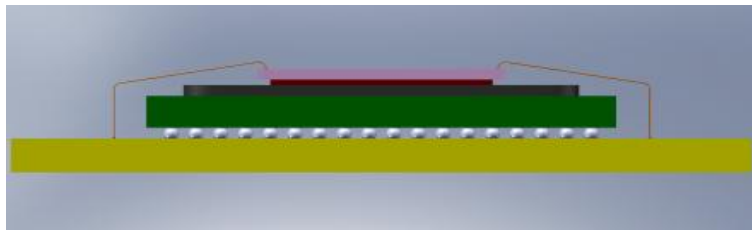
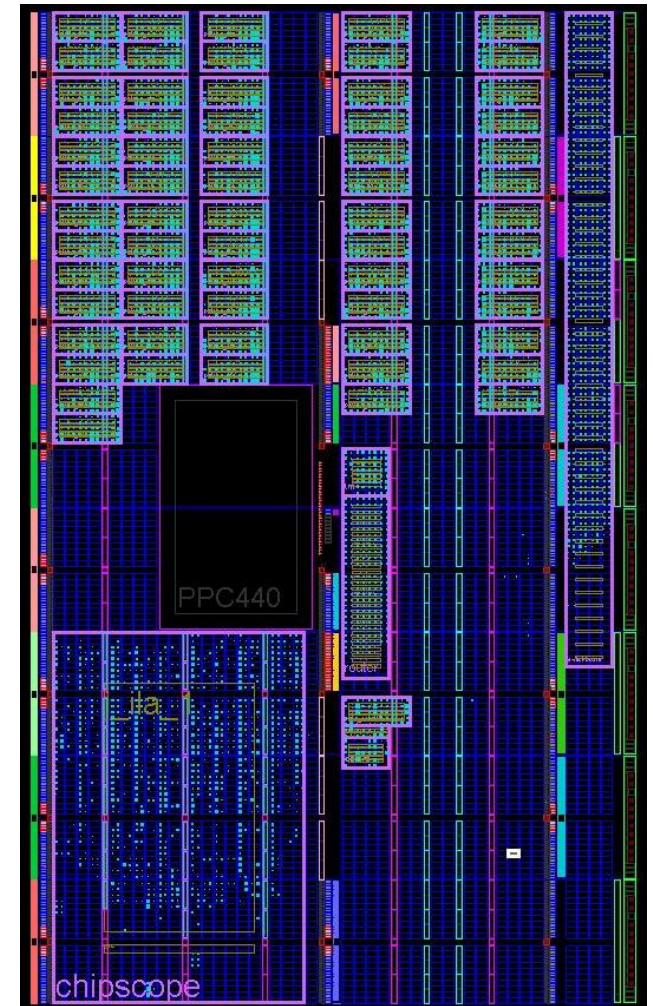
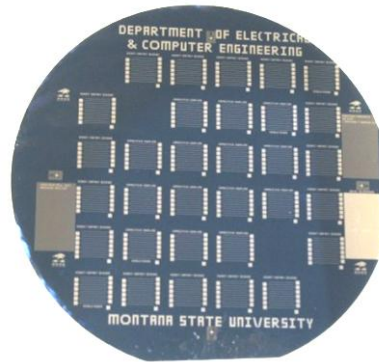
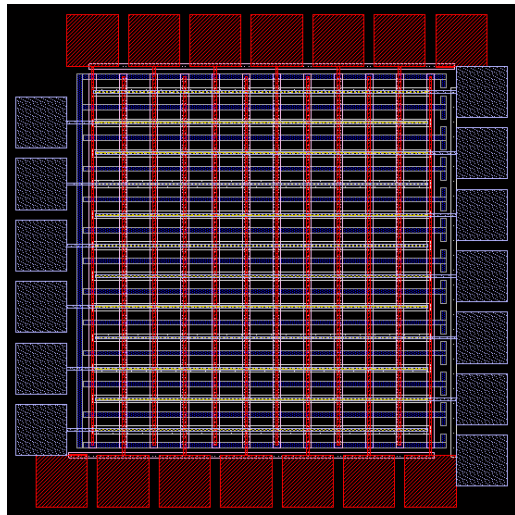
What happens during a recovery?

- Processors must be rebooted, reinitialized, and resynched



Our Approach

Integrated Sensor Can Be Coupled with FPGA For More Robustness





Questions

