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Impedance Matching Techniques for VLSI Packaging

Brock J. LaMeres, Agilent Technologies, Inc.

Rajesh Garg, Texas A&M University

Kanupriva Gulati, Texas A&M University

Sunil P. Khatri, Texas A&M University

Abstract

Impedance discontinuities caused by VLSI packaging are one of the largest challenges facing system level designers in the next decade. Modern IC process capability is exceeding the electrical performance of current packaging technology. The speed of the risetimes available on the IC cause the interconnect of the package to be treated as a transmission line. As a result, impedance discontinuities in the package will cause reflections which may result in intermittent switching of digital signals and edge time degradation, both of which limit system performance. The impedance discontinuity in the package is due to excess inductance and capacitance of the physical interconnect. To compensate for this problem, capacitance or inductance can be placed near the interconnect to alter its effective impedance over a given frequency range. This technique has been proven in microwave applications to match impedances at a known frequency. This paper presents the application of this impedance matching technique for use in broadband digital signals that are seen in modern VLSI designs. Two approaches are presented, a static compensation and a dynamic compensation. The static compensator places pre-defined capacitance or inductance on the package and on the IC to surround the parasitics of the interconnect. The dynamic compensator places a switch-able capacitance or inductance on the IC that can be programmed to a desired value to overcome design and manufacturing variations in the interconnect. Both techniques presented are shown to bound the reflections of the interconnect to less than 5% (down from 20% for an uncompensated structure) for the two most common types of interconnect used in VLSI packages (wire bond and flip-chip). In addition, both circuits utilize less area than an interconnect pad, making them ideal for placement directly beneath the pads.

Author(s) Biography

Brock J. LaMeres works as an R&D engineer in the Design Validation Division for Agilent Technologies in Colorado Spring. LaMeres has been part of Agilent for the past 7 years where he works on logic analysis probing and acquisition systems. LaMeres received his Ph.D. from the University of Colorado 2005 where his research focus was noise reduction techniques in IC packaging. He has published over 30 articles in the area of signal integrity and has been issued a patent in the field of logic analyzer probing. LaMeres is a registered Professional Engineer in the State of Colorado.

Sunil P. Khatri is an Assistant Professor in the Department of Electrical Engineering at Texas A&M University. He is affiliated with the VLSI CAD group. He completed his Ph.D. from the University of California, Berkeley in 1999. Before this, he worked with Motorola, Inc on the designs of the MC88110 and PowerPC 603 RISC Microprocessors. Khatri obtained his M.S from the University of Texas at Austin, which followed his B.Tech. from the Indian Institute of Technology, Kanpur. His research is in the areas of VLSI Design and VLSI CAD. Some recent areas of interest are design automation for datapath circuits, cross-talk avoidance in on-chip buses, leakage-power reduction, extreme low power circuit design, asynchronous circuit design methodologies, timing estimation, efficient test generation, fast logic simulation and cross-talk immune VLSI design.

Kanupriva Gulati is currently working on her MSEE at Texas A&M University in College Station, TX. Her research focus is on logic synthesis techniques for leakage computation, hierarchical don't care computation and BDD-based synthesis of structured ASICs. Kanupriya has a B.S. from the Delhi College of Engineering, India.

Rajesh Garg is currently working on his MSEE at Texas A&M University in College Station, TX. His research focus is on radiation-tolerant circuit design and pass transistor logic. Rajesh obtained his B.S. from the Indian Institute of Technology, Delhi, India.

I. Introduction

Wire bonding is the most commonly used methodology to connect signals from a silicon die to corresponding pads on a package substrate. Wire bonding is a fast and inexpensive process, which explains its popularity. While this technology has been refined over the years to provide a robust and inexpensive mechanical connection, the electrical parasitics associated with wire bonding are becoming a serious problem at today's data rates. Wire bonds tend to be highly inductive due to their large current return loops and distance from other conductors. As a consequence, wire bonds tend to have a higher impedance than the traditional 50Ω traces used for packages and for printed wiring boards (PWB's). The following expression gives the characteristic impedance of a loss-less transmission line and is used to model the impedance of the wire bond structure.

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

The wire bond is the largest source of excess inductance in the package [1] and causes unwanted signal reflections. Reflections on the transmission line are dictated by the reflection coefficient Γ.

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2}$$

The magnitude of the reflected signal is given by:

$$V_{reflected} = V_{incident} \cdot \Gamma \tag{3}$$

while the magnitude of the transmitted signal is given by:

$$V_{transmitted} = V_{incident} \cdot (1 - \Gamma) \tag{4}$$

These equations illustrate that any impedance mismatch due to a wire bond will result in reflected energy in addition to limiting the energy transmitted to the receiver.

As data rates of digital systems continue to increase, the speed limitations due to wire bonds are becoming a dominant factor in system performance. More advanced interconnect is available such as flip-chip bumping which can reduce the inductance present in the Level 1 (IC to Package) interconnect [1]. Flip-chip bumping is more costly than wire bonding but is an attractive option when performance is the leading design constraint. However, even flip-chip bumps contain inductive parasitics relative to a 50Ω system. Any technique that can increase the throughput of a VLSI package without moving toward non-standard processes will greatly assist in keeping the packaging cost down as speeds increase.

In this paper, we present techniques to alter the impedance of the level 1 interconnect by adding capacitance or inductance near the structure. For this work, the wire bond is considered the largest source of level 1 inductance that a designer will have to deal with. The first technique is a static capacitive

compensation in which capacitance is added to the package and on the IC near the wire bond pads. In order to prevent increased cost, embedded capacitors (EC) are used in the package substrate based on standard printed wiring board (PWB) processes. Embedded package capacitors are ideally suited to be implemented directly beneath the wedge bond pads on the package substrate [2], [3].

Two types of on-chip capacitors were evaluated for performance and area efficiency. The first is a Metal-Insulator-Metal (MIM) capacitor which is implemented in the upper metal layers of the IC. The MIM capacitor has the advantage that its value is independent of bias voltage [4]. However, its density is less than other on-chip capacitor techniques which increase its relative area. The second type of on-chip capacitor that was evaluated was a device-based structure. This type of capacitor, (also known as a PolySilicon capacitor) is implemented using the diffusion regions of the IC. This capacitor has a much higher capacitance density over the MIM capacitor, but suffers from bias voltage variation due to the semiconductor properties of the implementation [5].

The second impedance matching technique is a dynamic capacitive compensator. In the dynamic compensator, a programmable circuit is implemented on-chip that will switch in different values of capacitance to the wire bond pad. The circuit consists of CMOS pass gates that selectively connect different values of on-chip capacitance to the wire bond pad. The parasitics of the pass gates are considered in the calculation of the total excess capacitance that is switched in to compensate for the wire bond inductance. The circuit is designed to have enough compensation range to cover all reasonable lengths of wire bonds [1]. In addition, the programmability of the capacitance negates any process variation since the capacitance can be "dialed in" after IC fabrication and packaging. As with the static compensator, two types of on-chip capacitance were evaluated for performance and area (MIM and Device-based).

The third impedance matching technique is a static inductive compensator. In this compensator, spiral inductors are placed on-chip to raise the impedance of structures that have a lower impedance than the system ($Z_L < Z_0$).

We demonstrate that the capacitive techniques can successfully compensate for wire bond lengths up to 5mm using either the MIM or Device-based capacitors. Experimental results show that for rise times up to 117ps (equivalent to 3GHz using the risetime-bandwidth product rule [6]), the compensators can bound the impedance discontinuity to $<5\%$. This compares to discontinuities of up to 20% for uncompensated 5mm bond wires. In addition, the impedance of the compensated structure can be held to within 10Ω's of design (typically 50Ω's) to a much higher frequency. For a 3mm wire bond length, whose impedance strays to +/- 10Ω's at 3.1GHz, can be held to within tolerance up to 4.8GHz using a static compensator and up to 6.8 GHz using a dynamic compensator. In addition, the inductive techniques are able to compensate for flip-chip bumps which reside in a 125Ω system and bound reflections to 2% up to frequencies of 10GHz.

The rest of this paper is organized as follows. Section II presents previous work in the area of capacitor and inductor implementations that are used in our compensators. Section III describes the methodology used to achieve the impedance match. Section IV presents the electrical parameter extraction results for the package geometries studied in this work. Sections V and VI describe the design of the static and dynamic capacitive compensators respectively. Section VII describes the design of the inductive compensator design. Experimental results are given in Section VIII and conclusions drawn in Section IX

II. Previous Work

A. PWB Embedded Capacitors

There has been much work done to improve the electrical performance of capacitors on printed wiring boards. The main goal of the improvements is to increase the capacitance density and to reduce the equivalent series inductance. This improves the frequency performance of the capacitors for application in decoupling and impedance matching networks.

Work done in [7] and [8] showed an implementation of an embedded film capacitor (EFC) using standard copper clad lamination. A standard dielectric material was used (FR-4) with a dielectric constant 4.6. The capacitor's effectiveness was compared to that of 16 discrete capacitors in the application of power/ground plane impedance reduction. It was found that the ESL using the best EFC configuration was reduced to 106pH from 270pH when using 16x100nF discrete decoupling capacitors.

Additional improvement to embedded capacitors was illustrated in [2] for use in low-cost organic PWB's. In this case, polymer-ceramic nanocomposite materials were used to achieve high k (25-50) thin films. The photoimageable polymer-ceramic material has a low processing temperature ($< 200^{o}$C) which could be applied to a standard PWB process. The thickness of the EFC's was varied from $25um$ to $50um$. The authors reported a 20x reduction in SSN over a traditional PWB.

A more advanced high k material was presented in [9]. This work presented a hydrothermal barium titanate thin film to create EFC's. This process is attractive due to its low temperature processing ($< 160^{o}$C) and ability to be integrated onto organic PWB's. The process achieved extremely high k values (> 350) with capacitance densities of $1uF/cm^2$. The EFC's reported a 30% reduction in SSN over a frequency range from 0.01MHz to 500MHz.

All of these works lay the foundation for a low-cost embedded PWB capacitor implementation using standard process technology.

B. On-Chip Embedded Capacitors

There has also been work done to integrate high-density on-chip capacitors for use in decoupling power supplies. The goal of this type of decoupling is to compensate for the inductance in the level 1 interconnect to reduce SSN.

Metal-Insulator-Metal (MIM) capacitors were analyzed in [4] and [10] to study the effect of common on-chip insulator materials on the capacitance density. In this work the authors demonstrated fabrication of MIM's using three different dielectric materials (Oxide, Nitride, and Oxy-nitride). Over an acceptable range of thicknesses, the dielectrics studied produced capacitance densities from $1.4fF/um^2$ to $2.8fF/um^2$. These numbers exceeded the MIM standard of $1fF/um^2$. This work demonstrated the feasibility of implementing high-density on-chip capacitors using both $90nm$ and $0.13um$ CMOS process steps.

In [3] it was illustrated that active circuitry could be integrated directly beneath the wire-bond pads. It was demonstrated that ring-oscillator circuits in a $0.13um$ CMOS process suffered no noticeable degradation in gate delay or cycle time from being placed directly beneath the pads. Gate delays of

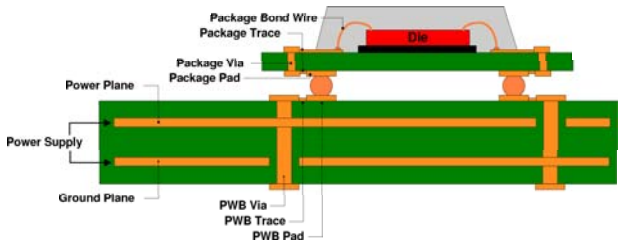

Fig. 1. Interconnect for BGA Package using Wire Bond

the structures beneath the bond pads matched very closely with the delays measured at the center of the die. While this technology was not explicitly noted for use in decoupling, the proximity to the inductance of the wire-bond makes it ideal for achieving a non-distributed decoupling or matching network. This technology lends itself well to implementing device capacitors directly beneath the wire-bond pads.

For this work, MIM-based and Device-based on-chip capacitors are used in the compensator designs. In each case, it is assumed that the capacitors are implemented directly beneath the wire bond pad to achieve the closest proximity to the wire bond inductance.

C. On-Chip Spiral Inductors

Spiral inductors are becoming a standard building block on-chip. As IC feature sizes shrink, the number of inductor turns that can be created in a reasonable area has increased. Now reasonable values of inductors can be implemented without considerable area requirements on the IC substrate [11]. The inductance of the spiral structures is dictated by the number of turns in the spiral in addition to the spacing and width of the traces that make up the spiral [12]. The main drawback of on-chip inductors is the excess capacitance and resistance that is present in the implementation. These parasitics result in a lowering of the quality factor (Q) of the inductor and must be included in the circuit analysis when using spiral inductors.

III. Methodology

In order to alter the impedance of the level 1 interconnect, excess capacitance or inductance is added near the structure. The process is the same whether adding capacitance or inductance to lower (or raise) the impedance. This section will describe the technique in terms of capacitive impedance compensation.

To reduce the impedance of the wire bond structure, excess capacitance must be added near the wire bond. The excess capacitance (C_{comp}) needed to match the wire bond structure to 50Ω's can be derived from equation 1 and is given by:

$$C_{comp} = \frac{L_{wb}}{50^2} - C_{wb} \tag{5}$$

Figure 1 shows the cross-section of a wire bonded, ball grid array (BGA) package. This figure shows the entire interconnect path from the IC substrate to the motherboard PWB traces. In this cross-section, the wire bond constitutes the largest source of excess inductance and therefore the largest impedance discontinuity in the system.

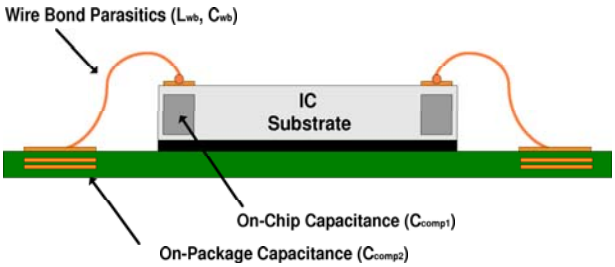

Fig. 2. Location of Compensation Capacitors and Wire Bond Parasitics

A. *Compensator Proximity*

In order to model the wire bond inductance and compensation capacitance as a single lumped element, the compensation capacitance must reside within a certain proximity of the wire bond. The maximum distance of the capacitance from the wire bond depends on the frequency components present in the digital signal. If the compensation capacitance resides close to the wire bond, the resulting structure can be modeled as a lumped element for much higher frequencies. For this work, a 117ps rise time (equivalent to 3GHz using the risetime-bandwidth product rule [6]) is used to evaluate the compensators. This rise time is sufficient to model the majority of inter-chip busses present today [1].

Typically, a structure is considered a lumped element when its electrical length (i.e. its propagation delay) is less than 20% of the highest rise time in the system [13]. Using a 117ps risetime and a worst case dielectric constant of silicon nitrate (ϵ_r=7) to determine the electrical length of an integrated structure, the acceptable proximity of the compensation capacitance to the wire bond can be found. For this work it is found that the compensation capacitance must be within 2.6 mm of the wire bond [6] for it to be accurately modeled as a lumped impedance for a 117ps rise time. From the work cited in Section II, it is shown that capacitor elements can be implemented directly beneath the wire bond pads on the package and on-chip. This is the optimal electrical location for the capacitors in addition to being the least spatially intrusive.

The first compensation capacitor location is beneath the wire bond pad on-chip (C_{comp1}). This capacitance is implemented using either a MIM-based or Device-based component. The second location is beneath the wire bond pad on the package substrate (C_{comp2}). This capacitance is implemented using an embedded parallel plate structure. Figure 2 show the location of the compensation capacitors.

B. *Static Compensation*

In the static compensator methodology, capacitance is placed on-chip (C_{comp1}) and on-package (C_{comp2}). The term *static* indicates that the capacitance that is added is of a pre-defined value. The capacitance values chosen are based off of the package design and the resulting wire bond parasitics. The variation in wire bond process must be considered in the selection of the capacitor values. The static compensator has the advantage that capacitance can be placed on both sides of the wire bond inductance. This has the effect that the wire bond and compensation structure appears more of a lumped element.

In the static compensator, the net compensation capacitance is given by:

$$C_{comp} = C_{comp1} + C_{comp2} \tag{6}$$

Using equation 1 to describe the impedance of the statically compensated structure, the impedance of the wire bond becomes:

$$Z_{0-static} = \sqrt{\frac{L_{wb}}{C_{wb} + C_{comp1} + C_{comp2}}} \tag{7}$$

C. Dynamic Compensation

In the dynamic compensator methodology, capacitance is only placed on-chip (C_{comp1}). The term *dynamic* means that the capacitance is programmable through active circuitry. The dynamic programmability of the compensation capacitance allows the compensator to successfully impedance match across variations in the wire bond inductance. The programmability means that the designer does not need to know the exact wire bond inductance prior to IC fabrication. This has the advantage that the dynamic compensator can accommodate process and design variation.

In the dynamic compensator, the net compensation capacitance is given by:

$$C_{comp} = C_{comp1} \tag{8}$$

Using equation 1 to describe the impedance of the dynamically compensated structure, the impedance of the wire bond becomes:

$$Z_{0-dynamic} = \sqrt{\frac{L_{wb}}{C_{wb} + C_{comp1}}} \tag{9}$$

IV. Electrical Modeling

The first step in designing the compensation networks is to model the electrical parameters of the structure making up the package interconnect.

A. Wire Bond Interconnect Modeling

For the wire bonded package in this work, we use a $5mm$ x $5mm$, wire-bonded silicon die that is mounted to a 22x22, $1mm$ pitch BGA package. The package uses a $1.27mm$ thick $GETEK^{©}$ substrate with traces designed to be 50Ω's using trace widths of $0.1mm$. The package is mounted to a $200mm$ x $250mm$ main PWB through standard controlled collapse solder ball technology. The main PWB uses a $1.575mm$ thick $GETEK^{©}$ substrate with traces designed to be 50Ω's using trace widths of $0.127mm$.

The connection from the silicon die to the package substrate is formed using standard wire-bond technology. The wire bond is a gold wire with a diameter of $25um$. The connection to the die is made using a *ball bond* to a $100um$ x $100um$ aluminum pad. The connection to the package is made using a *wedge bond* to a $100um$ x $400um$ gold plated pad. The net length of the wire-bond was varied from $1mm$ to $5mm$. The wire bonds and planes that form the embedded capacitors were modeled using the $Raphael$ EM Field Solver [14].

B. Flip Chip Interconnect Modeling

For the flip-chip package in this work, the same size die and package is used as described above. However, instead of wire bonds, standard controlled collapse flip-chip bumps are used as the level 1 interconnect. The flip-chip bumps have a diameter of $400um$ and a collapsed height of $250um$.

C. On-Chip Capacitor Modeling

For this work, on-chip capacitors are implemented in two ways. The first type of on-chip capacitor is a Metal-Oxide-Metal (MIM) structure. In this work a MIM was implemented on layer 3 of a $0.1um$ CMOS process from BPTM [15]. The MIM that was modeled had an area of $100um$ x $100um$ with $t_{ox} = 600A^{\circ}$ and $\epsilon_r = 7$ (Si_3N_4). The MIM achieved $1.15fF/um$ with linear capacitance versus bias voltage. This type of capacitor is suited well for impedance matching on signal paths where the bias voltage changes widely.

The second type of on-chip capacitor is a device-based structure. This capacitor is created by connecting the source and drain of a NMOS transistor to ground and using the gate as the positive terminal of the capacitor. This type of capacitor has a very high density due to the thin plate separation (t_{ox}). For the $0.1um$ process used in this work [16], [17], [15], $t_{ox} = 25\mathring{A}$ with $\epsilon_r = 3.9$ (SiO_2). The drawback of this type of capacitor is its non-linearity with bias voltage. For the capacitor in this work, the value changed from $27pF$ to $138pF$ ($100um$ x $100um$) as the bias voltage changed from $V_G = 0v$ to $V_G = 1.5v$.

D. Package Capacitor Modeling

Within the package, the most cost effective design for the capacitor size needed is an embedded structure. The embedded capacitor within the package substrate is implemented using standard parallel plate structures. Within the package, the minimum plane to plane separation allowed under normal process is $0.051mm$. A 50Ω stripline transmission line is designed using a lower dielectic separation of h_{below}=$0.051mm$ and a upper dielectric separation of h_{above}=$0.279mm$. This type of construction yields a signal impedance of 50Ω's while also achieving the highest capacitance density allowed by process on the same layer. This construction yielded a plate to plate capacitance density of $420fF/mm^2$.

E. On-Chip Spiral Inductor Modeling

The on-chip inductors where implemented using standard spiral construction on layer 4 of a $0.1um$ CMOS process. Ground planes were formed on layers 2 and 6 above the spirals to reduce on-chip cross

talk to other metal layers. Layers 3 and 5 were left empty to reduce the capacitance from the spiral metal to the ground planes. A width and spacing of $0.3um$ was used for the spiral routing.

Table I lists the electrical parameters for the structures modeled.

Structure	$C_{density}$	$L_{density}$	Size	C_{total}	L_{total}	Z_0
Wire-Bond	26 fF/mm	569 pH/mm	1 mm	26 fF	0.569 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	2 mm	52 fF	1.138 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	3 mm	78 fF	1.707 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	4 mm	104 fF	2.276 nH	148 Ω
Wire-Bond	26 fF/mm	569 pH/mm	5 mm	130 fF	2.845 nH	148 Ω
Flip-Chip Bump	1.5 fF/um	1.3 pH/um	250 um	39 fF	0.323 nH	91 Ω
On-Chip MIM-Based Capacitor	1.15 fF/um^2	negligible	100umx100um	11.5 pF	negligible	N/A
On-Chip Device-Based Capacitor ($V_{GS} = 0v$)	2.7 fF/um^2	negligible	100umx100um	27 pF	negligible	N/A
On-Chip Device-Based Capacitor ($V_{GS} = 1.5v$)	13.8 fF/um^2	negligible	100umx100um	138 pF	negligible	N/A
On-Package Embedded Capacitor	420 fF/mm^2	238 fH/mm^2	0.5 mm x 0.5 mm	0.105 pF	59 fH	N/A
0.125 nH On-Chip Spiral Inductor ($Q = 0.174$)	0.190 $fF/turn$	20 $pH/turn$	6.25 turns	1.19 fF	0.125 nH	N/A
0.250 nH On-Chip Spiral Inductor ($Q = 0.221$)	0.207 $fF/turn$	31 $pH/turn$	8 turns	1.66 fF	0.250 nH	N/A
0.500 nH On-Chip Spiral Inductor ($Q = 0.281$)	0.195 $fF/turn$	41 $pH/turn$	12 turns	2.34 fF	0.500 nH	N/A

TABLE I

ELECTRICAL PARAMETERS FOR SYSTEM INTERCONNECT

V. STATIC CAPACITIVE COMPENSATOR DESIGN

Using the electrical parameters from Table I and equations 6 and 7, the values of C_{comp1} and C_{comp2} for the static compensator can be found. Table II lists the optimal capacitor values to match the wire bond inductances (Table I) to 50Ω's. Table III lists the corresponding sizes to implement the impedance matching capacitors.

$Length_{wb}$	C_{comp1}	C_{comp2}
1 mm	102fF	102fF
2 mm	208fF	208fF
3 mm	325fF	325fF
4 mm	450fF	450fF
5 mm	575fF	575fF

TABLE II

STATIC COMPENSATION CAPACITOR VALUES

$Length_{wb}$	$C_{comp1-MIM}$	$C_{comp1-Device}$	$C_{comp2-EC}$
1 mm	10μm x 10μm	2.7μm x 2.7μm	388μm x 388μm
2 mm	14μm x 14μm	3.9μm x 3.9μm	554μm x 554μm
3 mm	18μm x 18μm	4.9μm x 4.9μm	692μm x 692μm
4 mm	21μm x 21μm	5.8μm x 5.8μm	815μm x 815μm
5 mm	24μm x 24μm	6.5μm x 6.5μm	921μm x 921μm

TABLE III

STATIC COMPENSATION CAPACITOR SIZES

VI. Dynamic Capacitive Compensator Design

A. Circuit Description

The design of the dynamic compensator consists of CMOS pass gates that connect to integrated binary-weighted capacitors. In our design, there are three integrated capacitors that can be switched in (C_1, C_2 and C_3). This number can be increased, but our experiments indicate that sufficient resolution can be achieved using just three capacitors. Each of these capacitors use a pass gate to connect to the wire bond (Pass Gate #1, Pass Gate #2, Pass Gate #3). Each pass gate has a control signal which either connects / isolates the capacitors to / from the on-chip I/O pad, which is connected to one end of the wire bond. Figure 3 shows the schematic of the dynamic compensator design.

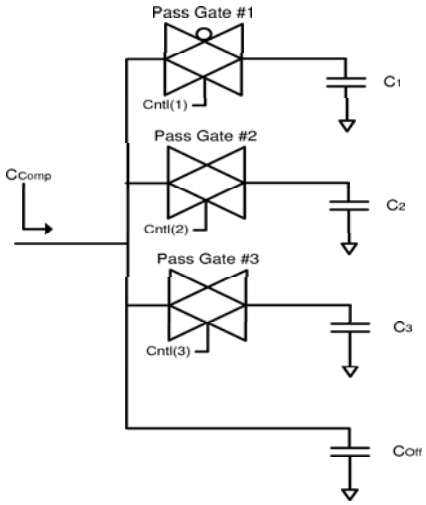

Fig. 3. Dynamic Compensator Circuit

B. Capacitor Design

The diffusion regions associated with the pass gates contribute an additional capacitance to C_{comp1}, which must be considered in the design. For each of the three programmable capacitor banks, the net capacitance will be the sum of the diffusion capacitance of the pass gate and the integrated capacitor. If the pass-gate of any bank i is turned off, then bank i simply contributes a capacitance C_{pgi} to C_{comp1}.

$$C_{Bank1} = C_{pg1} + C_1 \tag{10}$$

$$C_{Bank2} = C_{pg2} + C_2 \tag{11}$$

$$C_{Bank3} = C_{pg3} + C_3 \tag{12}$$

To achieve a programming range with uniform steps, the integrated capacitors are sized such that:

$$C_{Bank3} = 2 \cdot C_{Bank2} = 4 \cdot C_{Bank1} \tag{13}$$

Using three control bits, 8 programmable values of capacitance can be connected to the wire bond in increments of C_{Bank1}. To adjust the programmable capacitance to cover the desired compensation

range, C_{Off} is used. This capacitance is non-programmable and serves as an offset to set the minimum capacitance value of the compensator. Using the conventions just described, the range of the compensator can be described as:

$$C_{min} = C_{Off} = C_{pg1} + C_{pg2} + C_{pg3} \tag{14}$$

$$C_{max} = C_{Off} + C_{Bank1} + C_{Bank2} + C_{Bank3} \tag{15}$$

$$C_{step} = C_{Bank1} \tag{16}$$

In this work, the pass gates are implemented using a 0.1um CMOS process from BPTM [17], [18]. As with the static compensator, the integrated capacitors (C_1,C_2, C_3, C_{Off}) are implemented using two different on-chip techniques that are evaluated in this work (MIM-based and Device-Based). Both of these capacitor techniques are evaluated for range, area efficiency, and non-linearity for application in the dynamic compensator design.

C. Pass Gate Design

As described in the previous section, the pass gates will contribute to the total capacitance of each bank. The pass gate must be designed to have sufficient strength to drive the integrated capacitors (C_1, C_2, C_3). Typical CMOS design rules dictate that the pass gate sizing will be 1/3 of the size of an equivalent inverter that represents the integrated capacitor being driven [5]. This rule defines the amount of capacitance that will be present in each bank due to the pass gate and to the integrated capacitor.

$$C_{pg} = \frac{1}{3} \cdot C_{Bank} \tag{17}$$

$$C_{int} = \frac{2}{3} \cdot C_{Bank} \tag{18}$$

Using the equations 10-18 and the values from Table I , the sizing of the resulting compensation circuitry can be found. Table IV lists the values of the capacitors used in the dynamic compensator that will match the impedance of the wire bond to 50Ω's (equation 5).

$Length_{wb}$	C_{comp1}
1 mm	202fF
2 mm	403fF
3 mm	605fF
4 mm	806fF
5 mm	1008fF

TABLE IV
DYNAMIC COMPENSATION CAPACITOR VALUES

Table V lists the device sizes of the dynamic compensator circuit. The capacitances C_1, C_2 and C_3 are implemented as square devices for minimal area utilization. The total area of the compensator is the size of the equivalent enclosing square for the compensator. This equivalent square represents the *normalized* area for the circuitry. It is clear that the MIM-based dynamic compensator occupies more area than the Device-based compensator. However, the non-linearity of both compensators must be analyzed to compare the efficiency of the two circuits.

	MIM-Based	Device-Based
Component	Area (W × L)	Area (W × L)
Pass Gate #1	32.4μm x 0.1μm	32.4μm x 0.1μm
Pass Gate #2	62.5μm x 0.1μm	62.5μm x 0.1μm
Pass Gate #3	129.6μm x 0.1μm	129.6μm x 0.1μm
C_{off}	8.5μm x 8.5μm	2.5μm x 2.5μm
C_1	11μm x 11μm	3.3μm x 3.3μm
C_2	15.5μm x 15.5μm	4.6μm x 4.6μm
C_3	22μm x 22μm	6.6μm x 6.6μm
Total	65μm x 65μm	25μm x 25μm

TABLE V
DYNAMIC COMPENSATION CAPACITOR SIZES (NORMALIZED)

VII. STATIC INDUCTIVE COMPENSATOR DESIGN

To verify the effectiveness of an inductive compensation technique, spiral inductors are placed on-chip to compensate for the impedance of a standard flip-chip bump. Table I reports that the flip-chip bumps in this work have a characteristic impedance of 91Ω. Since this impedance is higher than the standard 50Ω used in the capacitive compensators, the flip-chip bumps will be matched to 125Ω instead. While 125Ω is not as common of an impedance, it illustrates the point of the inductive compensator.

Using the electrical parameters from Table I, the value of L_{comp} for the static inductive compensator can be found to match the structure to 125Ω. Note that the capacitance of the spiral inductor must be accounted for in the impedance calculation. Table VI lists the optimal inductor value and size to match the flip-chip impedance to 125Ω's.

Structure	L_{comp}	$Area_{comp}$
Flip-Chip Bump	0.32 nH	146μm^2

TABLE VI
STATIC COMPENSATION INDUCTOR VALUES

VIII. EXPERIMENTAL RESULTS

To evaluate the compensator design, SPICE [16] simulations were conducted on the system.

A. Static Capacitive Compensator Performance

In order to evaluate the performance of the static compensator, simulations were performed on all lengths of wire bonds listed in Table II. Figure 4 shows the simulated Time Domain Reflectrometry (TDR) of the static compensator (equation 3). A TDR simulation shows how much of a reflection (Γ) is caused by the wire bond. For each length of wire bond (1mm to 5mm), a 117ps (3GHz) input step is used to stimulate the wire bond. In figure 4, the TDR waveforms are offset in the voltage axis for view-ability with the 1mm curve on the top and the 5mm curve on bottom. For each length of wire bond the non-compensated, MIM-based, and Device-based static compensation curves are shown. This figure shows the dramatic reduction in wire bond reflections when using a static compensator. Table VII tabulates the reduction in reflections when using the static compensator(s).

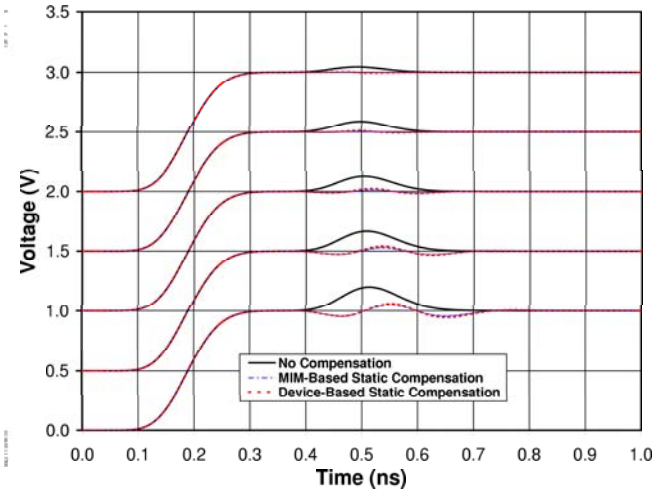

Fig. 4. Simulated TDR of Static Compensator

$Length_{wb}$	$\Gamma_{No-Comp}$	$\Gamma_{MIM-Comp}$	$\Gamma_{Device-Comp}$
1 mm	4.5%	0.05%	0.5%
2 mm	8.7%	0.4%	1.2%
3 mm	12.7%	1.3%	2.4%
4 mm	16.4%	2.7%	4.1%
5 mm	19.8%	4.8%	6.0%

TABLE VII
REFLECTION REDUCTION DUE TO STATIC COMPENSATOR

Another way to observe the effect of the compensator is to observe the input impedance of the structure in the frequency domain. Figure 5 shows the input impedance of the wire bond structure versus frequency for the 3mm wire bond. In this figure, the non-compensated, MIM-based, and Device-based static compensation curves are again shown. To compare the performance we record the frequency at which the input impedance moves to 10Ω's away from design ($f_{+/-10\Omega}$). In this case, the compensators are designed to match the structure to 50Ω's. This figure illustrates that adding a static compensator can keep the lumped impedance of the wire bond closer to 50Ω's up to a much higher frequency. In this case, the 3mm wire bond was kept to within 10Ω's of design up to 4.8GHz when using the MIM-based compensator (compared to only 3.1GHz when considering the un-compensated wire bond).

Table VIII lists the frequencies at which the input impedance strays to +/-10Ω's ($f_{+/-10\Omega}$) from design for all of the lengths of wire bonds evaluated.

$Length_{wb}$	$f_{No-Comp}$	$f_{MIM-Comp}$	$f_{Device-Comp}$
1 mm	9.3 GHz	14 GHz	12 GHz
2 mm	4.7 GHz	7.1 GHz	5.7 GHz
3 mm	3.1 GHz	4.8 GHz	3.8 GHz
4 mm	2.4 GHz	3.7 GHz	2.9 GHz
5 mm	1.9 GHz	3.0 GHz	2.5 GHz

TABLE VIII
$f_{+/-10\Omega}$ FROM DESIGN (STATIC COMPENSATOR)

These results show the dramatic reduction in impedance discontinuity when using a static compensator.

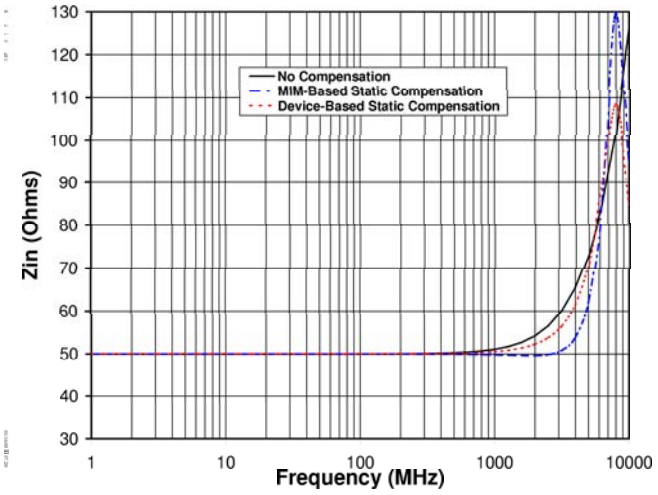

Fig. 5. Input Impedance of Static Compensator (3mm)

In all cases, the MIM-based compensator outperformed the Device-based compensator.

B. Dynamic Capacitive Compensator Performance

The same set of SPICE simulations were performed on the dynamic compensator to evaluate its performance.

1) Impedance Matching: Figure 6 shows the simulated TDR of the dynamic compensator (equation 3). Each length of wire bond (1mm to 5mm) is evaluated when stimulated with a 117ps (3GHz) input step. Again, the TDR waveforms are offset in the voltage axis for view-ability with the 1mm curve on the top and the 5mm curve on bottom.

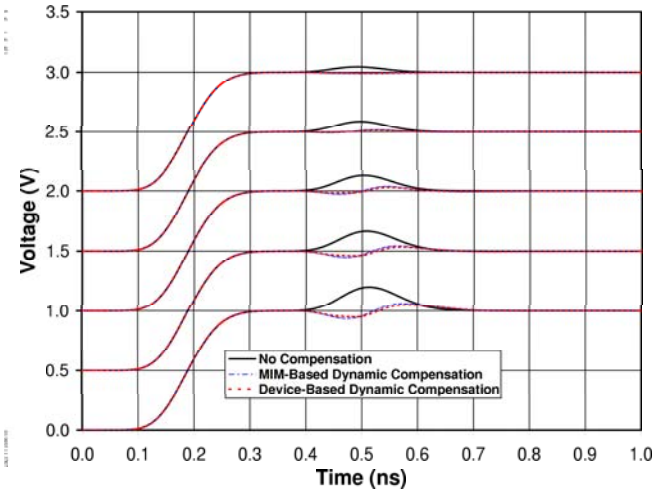

Fig. 6. Simulated TDR of Dynamic Compensator

Table IX tabulates the reduction in reflections when using the dynamic compensator(s), along with the binary setting used for the compensation.

$Length_{wb}$	$\Gamma_{No-Comp}$	$\Gamma_{MIM-Comp}$	$\Gamma_{Device-Comp}$	Setting
1 mm	4.5%	1.0%	1.0%	001
2 mm	8.7%	1.8%	1.3%	011
3 mm	12.7%	3.6%	3.0%	100
4 mm	16.4%	4.3%	3.3%	110
5 mm	19.8%	6.0%	5.0%	111

TABLE IX

REFLECTION REDUCTION DUE TO DYNAMIC COMPENSATOR

Figure 7 shows the input impedance of the wire bond structure versus frequency for the 3mm wire bond using the dynamic compensator. Once again, adding a compensator can keep the lumped impedance of the wire bond closer to 50Ω's up to a much higher frequency. In this case, the 3mm wire bond was kept to within 10Ω's of design up to 6.8GHz when using the Device-based compensator (compared to only 3.1GHz when considering the un-compensated wire bond).

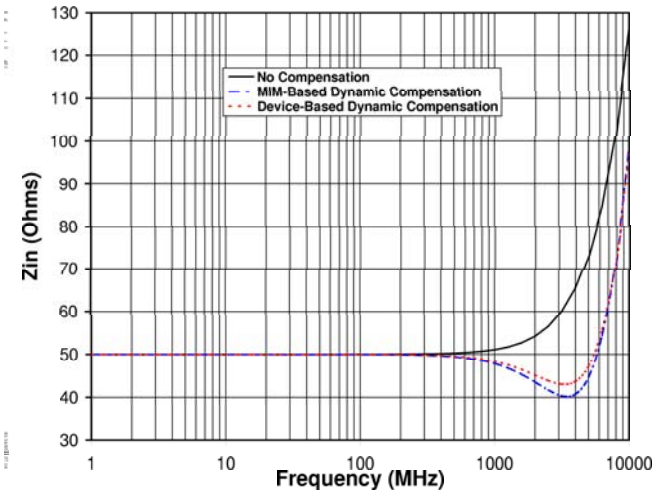

Fig. 7. Input Impedance of Dynamic Compensator (3mm)

Table X lists the $f_{+/-10\Omega}$ frequencies for all of the lengths of wire bonds evaluated using the dynamic compensator.

$Length_{wb}$	$f_{No-Comp}$	$f_{MIM-Comp}$	$f_{Device-Comp}$
1 mm	9.3 GHz	20 GHz	20 GHz
2 mm	4.7 GHz	10.1 GHz	10 GHz
3 mm	3.1 GHz	6.8 GHz	6.7 GHz
4 mm	2.4 GHz	5.2 GHz	5.1 GHz
5 mm	1.9 GHz	4.2 GHz	4.1 GHz

TABLE X

$f_{+/-10\Omega}$ FROM DESIGN (DYNAMIC COMPENSATOR)

2) Compensator Range and Linearity: Due to the non-linearity of the Device-based capacitors and active pass gates, the linearity of the dynamic compensator was evaluated to ensure the desired range was being reached. For each dynamic compensator setting, the bias voltage was changed for $V_G = 0v$ to $V_G = 1.5v$ and the corresponding capacitance was recorded. Table XI lists the effect of bias voltage on both the MIM-based and Device-based compensator circuits. This clearly shows the non-linearity of the

		MIM-Based Compensator			Device-Based Compensator		
Compensator Setting	$C_{(desired)}$	$C_{(V_{bias}=0v)}$	$C_{(V_{bias}=1.5v)}$	$C_{average}$	$C_{(V_{bias}=0v)}$	$C_{(V_{bias}=1.5v)}$	$C_{average}$
001	200 fF	252 fF	262 fF	257 fF	222 fF	281 fF	251 fF
010	325 fF	373 fF	382 fF	378 fF	318 fF	414 fF	366 fF
011	450 fF	499 fF	540 fF	519 fF	423 fF	587 fF	505 fF
100	575 fF	588 fF	596 fF	592 fF	485 fF	651 fF	568 fF
101	700 fF	713 fF	754 fF	734 fF	592 fF	816 fF	704 fF
110	825 fF	828 fF	895 fF	862 fF	688 fF	968 fF	828 fF
111	950 fF	948 fF	1041 fF	994 fF	788 fF	1180 fF	984 fF

TABLE XI

DYNAMIC COMPENSATOR RANGE AND LINEARITY

Device-based compensator which experiences as much as 33% capacitance variation when programmed to its maximum setting. This variation matches expected variation of standard CMOS PolySilicon gate capacitors [5]. Note that the MIM capacitors also exhibit variability, which occurs due to the bias dependence of the pass gate diffusion capacitances [19]. While both dynamic circuits experience bias voltage dependence, the compensators had sufficient range to cover wire bond lengths from 1mm to 5mm.

These results illustrate that the Device-based compensator outperformed the MIM-based compensator when implemented in a dynamic architecture. Also, both dynamic compensators outperformed the static compensators.

C. Inductive Compensator Performance

Figure 8 shows the simulated TDR plot of a flip-chip package being matched to 125Ω using the inductive compensator. This plot shows that the uncompensated flip-chip interconnect results in a 2% reflection when placed in a 125Ω system. The addition of the on-chip inductive compensator bounds this reflections to less than 1%.

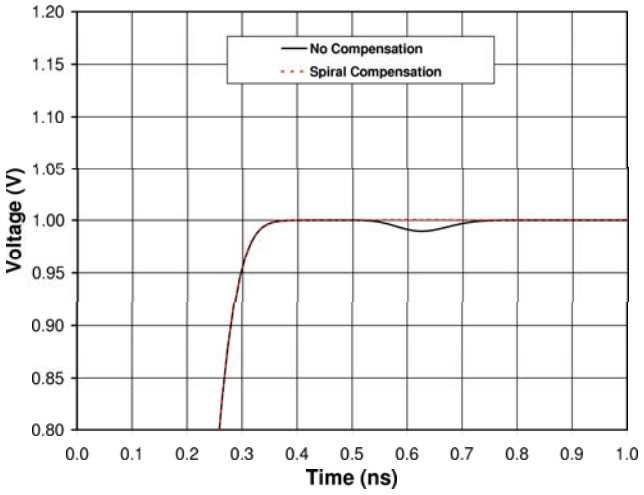

Fig. 8. Simulated TDR of Inductive Compensator

Figure 9 shows the input impedance of the flip-chip interconnect with and without inductive compensation. The impedance of the structure is shown to decrease starting at 2GHz due to the capacitive nature

of the parasitics. The inductive compensation holds the impedance of the interconnect to within 2Ω of design out to 10GHz.

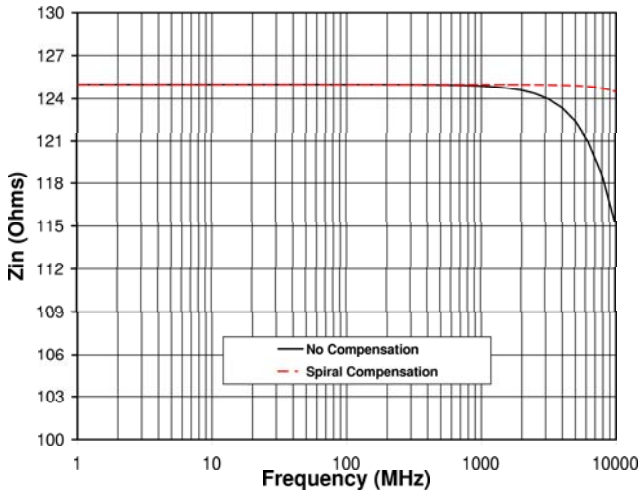

Fig. 9. Input Impedance of Inductive Compensator

D. Compensator Calibration

To program the compensator to the optimal impedance value, a calibration can be performed at package test.

The circuit used to perform the calibration is inspired by TDR ideas, but is simplified for applicability in a standard, low-cost VLSI tester setting. The calibration circuitry is simple and can be placed in the IC test equipment so that extra circuitry is not needed on the IC. In addition, pre-existing control logic and software interfaces in the tester can be used for calibration. Figure 10 shows the calibration circuitry for the compensator.

To measure the impedance discontinuity from the interconnect / compensator, the IC tester transmits a voltage step into the IC package. The magnitude of the reflection from the discontinuity is measured in the tester using comparator circuits. The comparator circuits are used instead of a standard A/D converter (as in a true TDR system) to reduce complexity and cost. One comparator monitors for reflections that exceed a user-defined Upper Control Limit (UCL). A second comparator monitors for reflections that exceed a Lower Control Limit (LCL). The programmable voltages are set by a Digital Control Monitor (DCM) in the IC tester.

When a reflection off of the interconnect/compensator element is above/below the violation limits, the comparator(s) will output a glitch signal that indicates a limit violation (V_UCL / V_LCL). The limit violation glitch is fed into the clock input of a D-flip-flop whose data input is tied to a logic 1. The D-flip-flop serves as a trigger element that will switch and remain high when it observes any glitch from the comparators. The D-flip-flop will remain high until reset by the DCM. The output of the two D-flip-flops are fed into an OR-gate to combine the upper and lower violation signals into one input (VIO) that is monitored by the DCM.

When the DCM observes a violation, it will communicate with the IC under test to change the

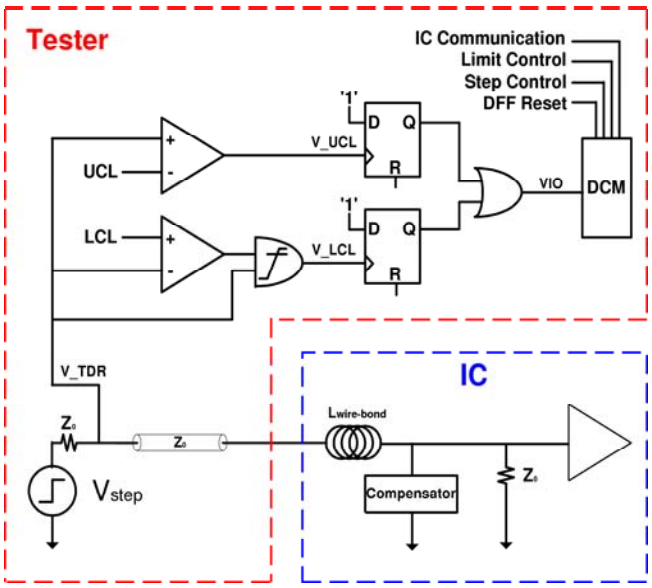

Fig. 10. Dynamic Compensator Calibration Circuit

compensator settings. Once the compensator is adjusted, the D-flip-flops are reset and another voltage step is launched into the IC package. This process is repeated until the magnitude of the reflections are within the LCL and UCL limits.

The lower control limit violation signal (V_LCL) is qualified using an AND-gate. The purpose of the AND-gate is to prevent glitches on V_LCL when the step voltage is below the LCL due to normal operating conditions such as the beginning of the rising edge of the step. The AND-gate is designed to have a high switch-point such that $V_{switchpoint-AND} >$ LCL. Once the step voltage exceeds the switch-point of the AND-gate, the glitches from the comparator are allowed to pass through to the D-flip-flop. Spurious glitches which may be observed when the step voltage is below the AND gate switch-point are thus filtered out, and the glitches at the output of the AND gate will therefore be solely due to reflections from the package (which violate the LCL).

In the case that the compensator cannot find a setting that meets the reflection control limits, it will relax the limit voltages going to the comparators. Using this technique, the minimum net reflection can be achieved by matching the positive and negative reflection magnitude of the interconnect/compensator. Since this calibration is only performed on the signal pins of the IC package, the overhead associated with the process is small. The calibration can be sped up further by setting the UCL and LCL to pre-defined values that are based on the design of the IC and package. If the tester uses reasonable limits to begin with, the convergence time of the algorithm will be reduced.

Figure 11 shows the signals of the calibration circuit during operation. In this case, the limits are set to indicate violations when reflections exceed 5%. In this figure an UCL violation is indicated by a glitch on V_UCL. The glitch then triggers the D-Flip-Flop which in turn sends a static control signal (VIO) to the DCM.

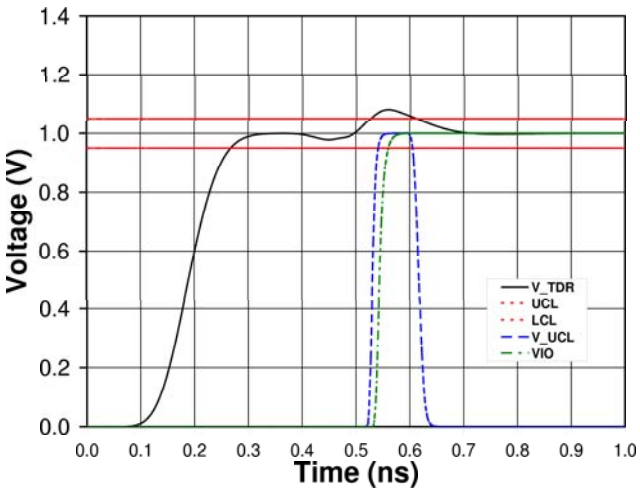

Fig. 11. Dynamic Compensator Calibration Operation

IX. Conclusion

This paper presented the design of compensation techniques for use in matching the impedance of package interconnect to the system impedance. The compensators placed capacitance or inductance near the level 1 interconnect to alter the structure's impedance. A static capacitive compensator was evaluated that placed pre-determined capacitance on both the package and on-chip to surround the wire bond inductance. A dynamic capacitive compensator was evaluated that placed programmable capacitance on-chip that could be changed to accommodate varying lengths of wire bonds. For both compensators, two types of on-chip capacitors were explored (MIM-based and Device-based). In addition, a static inductive compensator was evaluated that placed pre-determined spiral inductors on-chip to raise the impedance of the package interconnect.

All compensators significantly reduced the reflections due to the package interconnect discontinuity. In the case of the static capacitive compensator, the MIM-based on-chip capacitors outperformed the Device-based capacitors. In the case of the dynamic capacitive compensator, the Device-based on-chip capacitors outperformed the MIM-based. All compensators could be implemented in less area than a traditional wire bond pad which make them ideal for implementation directly beneath the pad structure.

The dynamic capacitive compensator outperformed the static compensator in all regards. The dynamic capacitive compensator was able to bound reflections to $<5\%$ for wire bond lengths up to 5mm (compared to as much as 20% for an uncompensated 5mm wire bond). In addition, the dynamic compensator held the input impedance to within 10Ω's of design up to 6.8 GHz compared to only 3.1 GHz for an uncompensated 3mm wire bond. The inductive compensator was shown to bound reflections for a flip-chip interconnect to less than 1% when residing in a 125Ω system.

For the dynamic compensator, the circuit description and design methodology were presented to appropriately size the pass gates and integrated capacitors. In addition, a calibration circuit and algorithm was presented that can be used at package test to find the optimal compensator setting for any wire bond inductance.

The compensators presented in this paper can be used to increase the throughput of packaging technologies as data rates increase. This technique will aid in keeping the cost of VLSI packaging down while still addressing the need for increased system performance.

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