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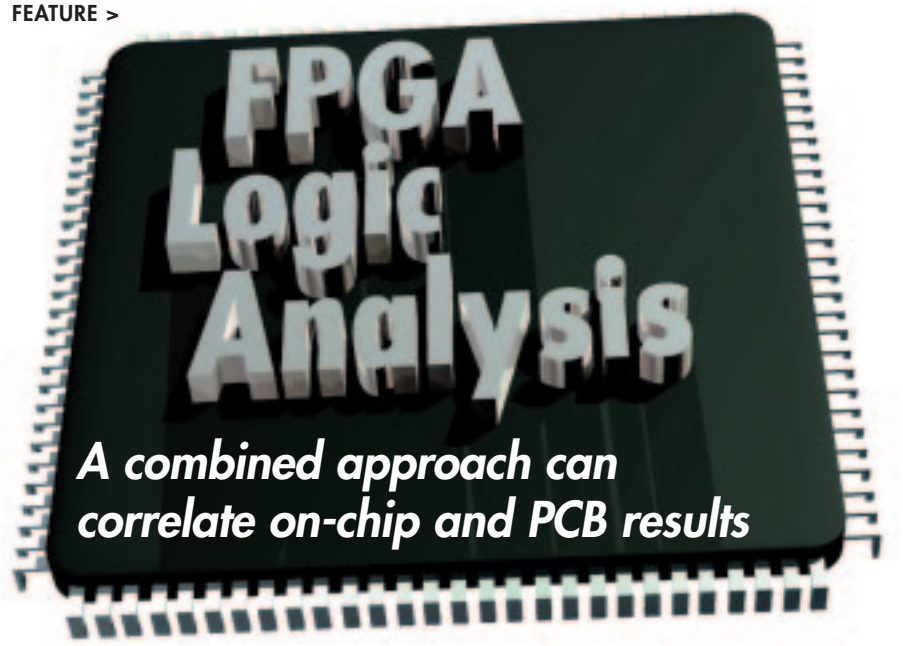

A combined approach can correlate on-chip and PCB results

By Brock J. LaMeres

Until recently, correlating on-chip signal integrity and functionality to the actual received signal on a printed circuit board has been difficult for engineers. Because certain points in a circuit are not accessible by standard test equipment, it has been very difficult to diagnose signal integrity or functional problems, with the results often being speculative. Consequently, engineers have relied heavily on computer modeling to gain pseudo-access to unattainable points in the circuit.

The combination of a benchtop logic analyzer and a logic analyzer software tool that can easily debug multimillion field programmable gate array (FPGA) designs is now addressing these engineering frustrations. Signals now can be observed simultaneously within an FPGA and on the PCB. This gives engineers access to two points in a circuit—one within the FPGA and one on the PCB—allowing them to quickly diagnose signal integrity and functional issues using empirical results.

This article will discuss current methods of analyzing circuits where test points are inaccessible, describe the roles and features of the logic analyzer and logic analysis software tool, and explore the advantages and disadvantages of each—as well as what their capabilities are when paired together to analyze what were once considered inaccessible test points. The article also will look at the output of this instrument duo, showing how the results will be the same, and provide a signal integrity example, explaining how the results would differ.

Current analysis methods

Currently, when engineers design a system that contains both FPGA functionality and high-speed PCB design, the two design tasks are de-coupled. The FPGA design is developed using logic simulators from companies such as Cadence Design Systems and SimuCAD. By using models of the gates within the FPGA, together with post-synthesis timing information, an engineer can get a first-order approximation of the design's speed and robustness. Meanwhile, the PCB is designed using analog simulators such as SPICE and IBIS.

By using the driver models of the FPGA and transmission line models of the PCB, an engineer can develop a transport system that has the necessary signal integrity for a given application. Unfortunately, when the system is realized, the two designs cannot be decoupled using standard test equipment.

Benchtop logic analyzers and oscilloscopes are the most common methods used to debug an actual system. When working with computer-type systems that contain high signal counts, the benchtop logic analyzer becomes the instrument of choice. Although a benchtop logic analyzer can provide engineers with high signal count, speed, and analysis tools, it still can only see one point in the circuit. If a signal is not received in the logic analyzer, this can be due to either a problem with the FPGA driver or a signal integrity issue on the PCB. The only method that's been available to engineers to diagnose this problem has been to use an oscilloscope and manually "comb" through the failed signals. However, the following solution now allows engineers to

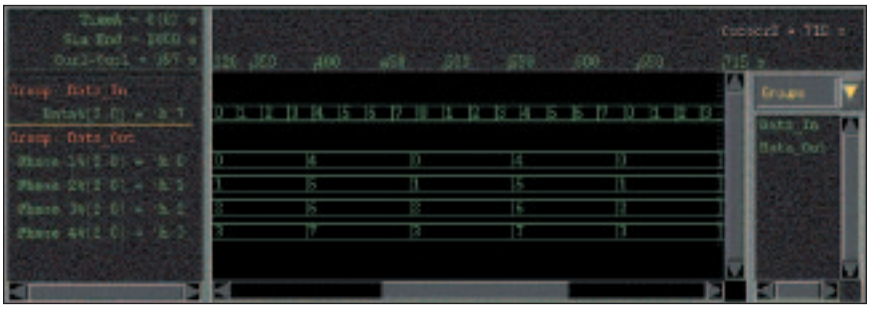

Figure 1 – Logic simulation results of a demux-by-4 circuit

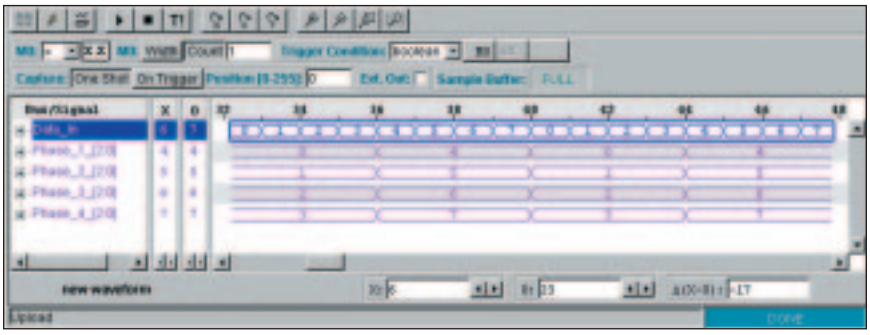

Figure 2 – Xilinx ChipScope acquisition results

diagnose the problem quickly without using an oscilloscope.

Benchtop logic analysis

A benchtop analyzer enables an engineer to probe high signal counts and correlate the data easily through advanced triggering and analysis tools. For example, Agilent Technologies' 1680A benchtop logic analyzer provides a quick, portable way to examine signals on the PCB and is capable of acquiring 128 channels of data in "STATE" mode at a clock rate of 200 MHz. The state clock can be comprised of any Boolean combination of four separate state clocks. In the "TIMING" mode, 136 channels of data can be acquired at a sampling speed of 800 MHz. Memory depths can extend to 2 megabits per channel.

As far as disadvantages are concerned, the sole failing of a benchtop analyzer is that it only monitors the signals at one point in the circuit. By doing this, the functional and signal integrity issues are not de-coupled.

On-chip logic analysis

The Xilinx ChipScope ILA is an integrated logic analyzer that is incorporated into a functional design prior to downloading it into the FPGA. This on-chip logic analyzer uses a small number of resources, and some of the dedicated memory blocks available to the user can provide up to 256 channels of data acquisition. Memory depth can extend up to 16 kilobits per channel with some devices. Any signal in the design can be probed with the analyzer. A trigger is defined prior to downloading. Once the data has been acquired, the empirical results can be downloaded directly to a PC using the joint test action group (JTAG) port of the FPGA. The results are then examined as waveforms on the PC, enabling engineers to *see* into the FPGA.

Engineers also have the ability to acquire data on internal nodes that were once inaccessible. Large numbers of signals can be monitored depending on the size of the design and available resources left for the analyzer. In addition to analyzing internal nodes, it also can monitor external nodes. Although this may seem redundant given the fact that benchtop logic analyzers can monitor external nodes as well, when these two analyzers are coupled together, they present a powerful duo capable of isolating functional and signal integrity issues simultaneously.

Simultaneous on-chip and PCB logic analysis

The primary advantage of pairing these two logic analysis systems together is to provide two points of a circuit to monitor across high channel counts. As a result, the functional and signal integrity issues are decoupled.

Engineers can start out with a low-speed measurement, and by correlating the on-chip results acquired by both logic analysis instruments, perform low-speed functional analysis on the system. At this level, engineers can determine whether their empirical results match their logic simulations. In addition, any DC driver errors that may be present due to circuit problems in the PCB transport system can be detected. Once low-speed operation is verified, the system can run at its target frequency. At high speeds, critical timing paths of the FPGA can be examined as well as signal integrity issues on the PCB.

Measurement results

To illustrate the power of this logic analysis duo, take a simple demux-by-4 circuit. This circuit will sample an input data stream and output each piece of data to one of four output nodes. The result is to create four synchronous output samples that are at one-fourth the input frequency—a common technique in data acquisition. **Figure 1** shows the logic simulation results that provide the "golden" reference to which the FPGA and PCB transport system will be compared. The data is grouped in a three-wide bus to use the hexadecimal values, and to more easily illustrate the demux operation.

Once the FPGA design is synthesized, the on-chip logic analyzer can be integrated into the design. At this point, the engineer can specify which signals to probe, as well as a trigger pattern and the acquisition depth. The combined pieces are then imple-

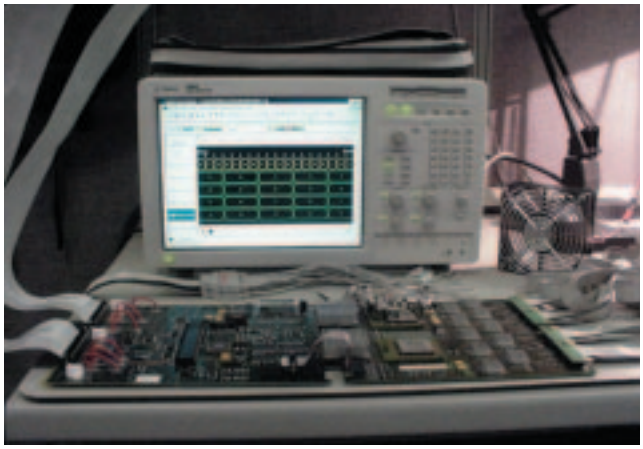

Figure 3 – Laboratory set-up using the Agilent 1680A benchtop logic analyzer

mented into a bit-stream and downloaded into the FPGA. A JTAG cable connects to the FPGA that controls the on-chip logic analyzer. The engineer then executes a "RUN" command on a PC, using integrated logic analyzer software to communicate to the on-chip analyzer to start acquiring data. Once the trigger pattern has been found, the data is transferred to the integrated logic analyzer tool through JTAG to be viewed as waveforms. **Figure 2** shows the on-chip logic analyzer acquisition results.

The second part of the analysis comes from the benchtop logic analyzer measurement. Using a 16-channel, flying lead probe set, the PCB outputs of the FPGA can be probed. **Figure 3** shows the laboratory set-up used to accomplish this measurement, while **Figure 4** displays the empirical waveform results of the data acquisition on the PCB. This demonstrates that both the benchtop analyzer and logic analyzer software tool have acquired the same data.

The following cases provide some examples of problems where engineers can use the logic analysis duo to debug.

CASE 1 - A functional problem within the FPGA

At the beginning of the debug process, the system runs at low speeds (i.e., <1 MHz). This isolates functional problems without introducing critical-path issues within the FPGA, or signal integrity issues on the PCB. A functional problem on the FPGA can be caused by a design error, or a synthesis/implementation error. For this type of problem, a benchtop logic analyzer and an on-chip logic analyzer each will have the same results, but differ when it comes to logic simulation. **Figure 5** shows the integrated logic analyzer results of a functional error within the FPGA.

CASE 2 - A DC problem on the PCB

Once the low-speed functionality of the FPGA has been verified, DC errors can be found on the PCB. In this case, the on-chip logic analyzer results will be correct, while those of the benchtop analyzer will be incorrect. At low speeds, a PCB problem is usually a DC error in the circuit. This can be caused by the driver's or receiver's impedance not being what it was originally designed to be. Another possibility is a misload of a termination resistor resulting in an over-attenuated signal swing. If the signal at the receiver is attenuated too much, the receiver may not be able to detect its logic level. Here, the benchtop analyzer's user-defined reference voltage is a useful tool for discovering this type of problem. **Figure 6**

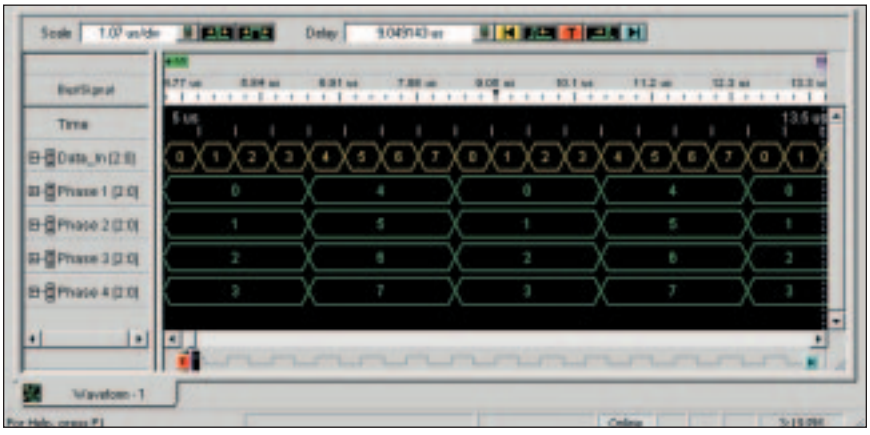

Figure 4 – *Acquisition waveforms from the Agilent benchtop logic analyzer*

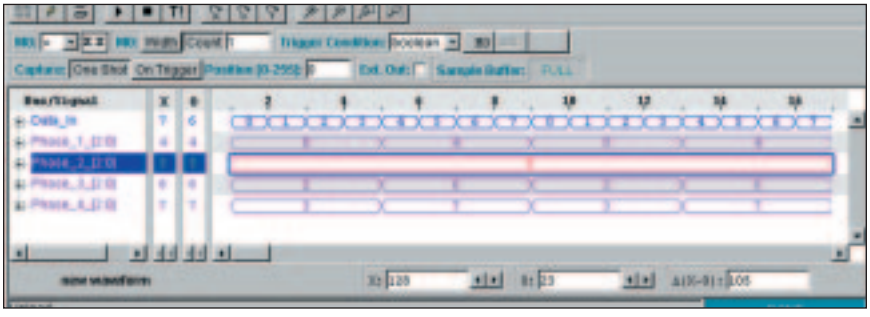

Figure 5 – *Xilinx ChipScope results monitoring a functional error within the FPGA*

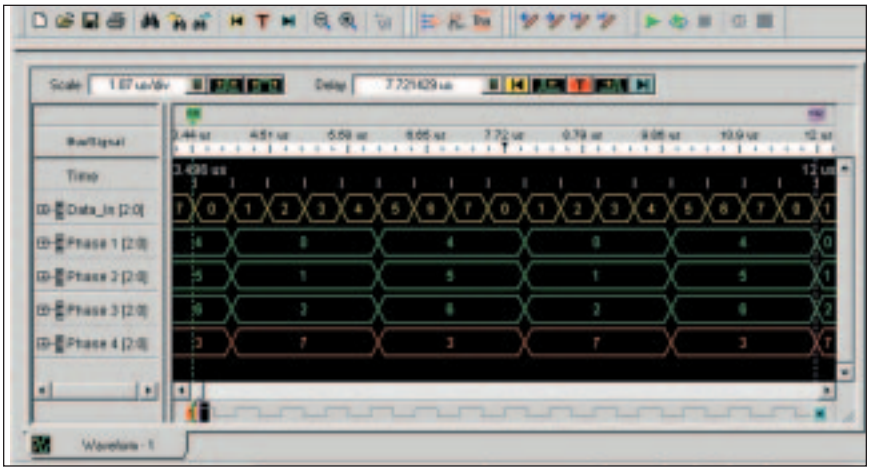

Figure 6 – *Agilent 1680A results monitoring a DC problem on the PCB*

TABLE 1 - Step-by-step debug process using the logic analysis duo

	Speed	ChipScope Results		1680A Results		Conclusion
		Match Logic Simulation?	Match 1680A?	Match Logic Simulation?	Match ChipScope?	
CASE 1	Low	No	Yes	No	Yes	Functional problem within the FPGA design
CASE 2	Low	Yes	No	No	No	DC problem on the printed circuit board
CASE 3	High	No	Yes	No	Yes	Timing issue within the FPGA design
CASE 4	High	Yes	No	No	No	Signal integrity issue on the printed circuit board

shows the results of monitoring a DC problem on a PCB with a benchtop analyzer.

CASE 3 – A high-speed failure within the FPGA

The next step in the debug process after verifying low-speed functionality of both the FPGA and the PCB is to look for high-speed faults since the system can now be run at or near its target frequency. The problem this time is a high-speed functional issue within the FPGA that can be caused by a critical path not meeting its timing requirement, or any other type of timing defect within the design. For this type of error, both logic analyzers will have the same results, but differ from the logic simulation performed. The FPGA design can be taken offline to rerun simulations to isolate the problem.

CASE 4 – A high-speed failure on the PCB

After the FPGA design has been resolved for high-speed operation, the PCB can be investigated for such problems as a high-speed PCB signal integrity error. This type of error can be caused by reflections, crosstalk, simultaneous switching noise, or ground bounce—to name just a few cases—and can be isolated with the benchtop logic analyzer. If, at high speeds, the integrated logic analyzer results match the logic simulation but not the benchtop logic analyzer, this indicates a signal integrity problem on the PCB.

Table 1 summarizes the step-by-step debug process presented in the four cases.

Conclusion

The combination of the two logic analyzer tools allow engineers to probe two points in a system, where previously only one was accessible. This new ability gives them a way to debug functional and high-speed problems simultaneously in the FPGA and on the PCB.

As signal counts within computer systems continue to increase, the logic analyzer is becoming the test equipment of choice for system engineers. In addition, as time-to-market becomes a more critical issue, the need for test equipment that can deliver faster results is assuming marked significance. The benchtop and on-chip logic analyzers are two pieces of test equipment that are meeting the demands of today's engineers. The combination of these two instruments provide a way for engineers to quickly diagnose and isolate FPGA and PCB problems that once could not be decoupled.

Brock LaMeres is currently a hardware design engineer for Agilent Technologies, where he designs high-speed printed circuit boards used in logic analyzers. He is also a part-time instructor in microprocessor systems at the University of Colorado in Colorado Springs. His research interests include modeling and characterization of transport systems and high-speed digital design. LaMeres received his B.S.E.E. from Montana State University, and his M.S.E.E. from the University of Colorado.